CMS32M57xx Reference Manual

Enhanced flash 32-bit motor microcontrollers

Rev. 1.0.7

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1. ARM Cortex–M0 core

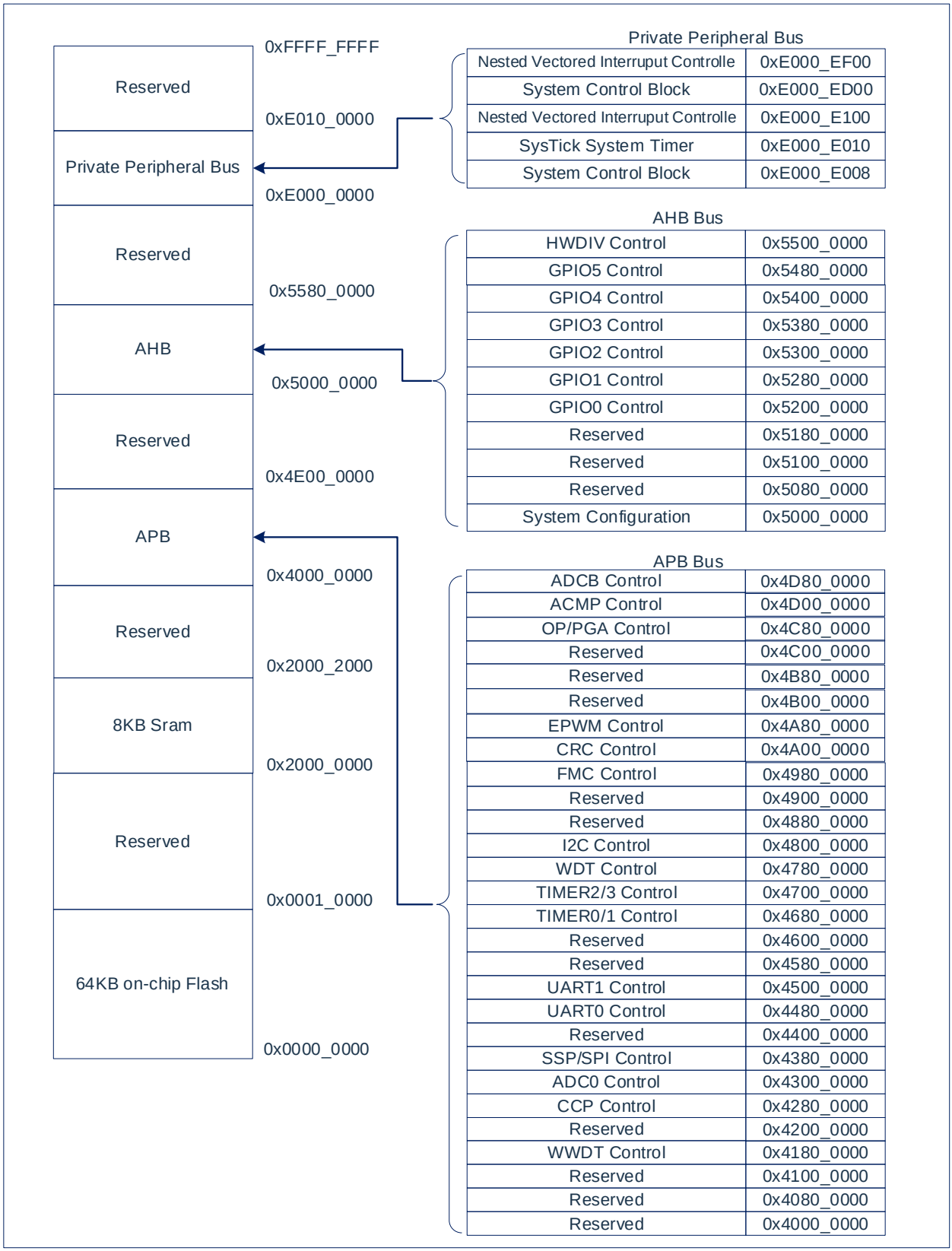
1.1 overview

The Cortex-M0® processor is a configurable, 32-bit RISC processor with multi-stage pipeline. It has an AMBA AHB-Lite interface and includes NVIC components, as well as optional hardware debugging capabilities. The processor can execute Thumb instructions and is compatible with other Cortex-M® series processors. The processor supports two modes of operation – Thread mode and Handler mode. When an exception occurs, the system enters Handler mode, and the exception return can only be performed in Handler mode. You can enter Thread mode after the system resets and the exception returns.

1.2 characteristic

- Low gate count processor:
  - ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - The ARMv6-M is compatible with 24-bit system timers.
  - A 32-bit hardware multiplier.
  - The system interface supports small-endian data access.
  - Accurate and timely interrupt handling capabilities.
  - Loading/storing multiple data and multicycle multiplication instructions can be terminated and then restarted for fast interrupt handling.
  - Exception compatibility mode for the binary interface of the C application.
  - ARMv6-M's C Application Binary Interface (C-ABI) exception compatibility mode allows users to implement interrupt handling using pure C functions.
- NVIC:
  - 32 external interrupts, each with a priority of 4.
  - Dedicated non-maskable interrupts (NDIs).
  - Both level and pulse trigger interrupts are supported.
  - Supports interrupt wake-up controllers (WICs) that provide very low-power idle modes.
- Debugging support:
  - Four hardware breakpoints.
  - Two observation points.
  - Program Count Sampling Register (PCSR) for non-intrusive code analysis.
  - Single-step and vector capture capabilities.
- Bus interface:
  - Provides a simple and integrated single 32-bit AMBA-3 AHB-Lite system interface for all system interfaces and memory.
  - Supports a single 32-bit slave port for DAP (Debug Port).

2. Storage mapping



Note: The above is the largest resource map for this series of products.

3. Clock control

3.1 overview

The clock controller provides a clock source for the entire chip, including the system clock and all peripheral clocks. The controller also controls power consumption through separate clock switches, clock source selection, and a divider.

The clock generator consists of the following two clock sources:

- Internal high-speed oscillator HSI (48MHz/64MHz).
- Internal low speed oscillator LSI (40KHz).

3.2 Feature description

3.2.1 Configure the CLKO feature

- Set the relevant port configuration register to the CLKO function.
- Set the CLKODIV register, select the clock source, and divide the output.
- Enables the CLKO output.

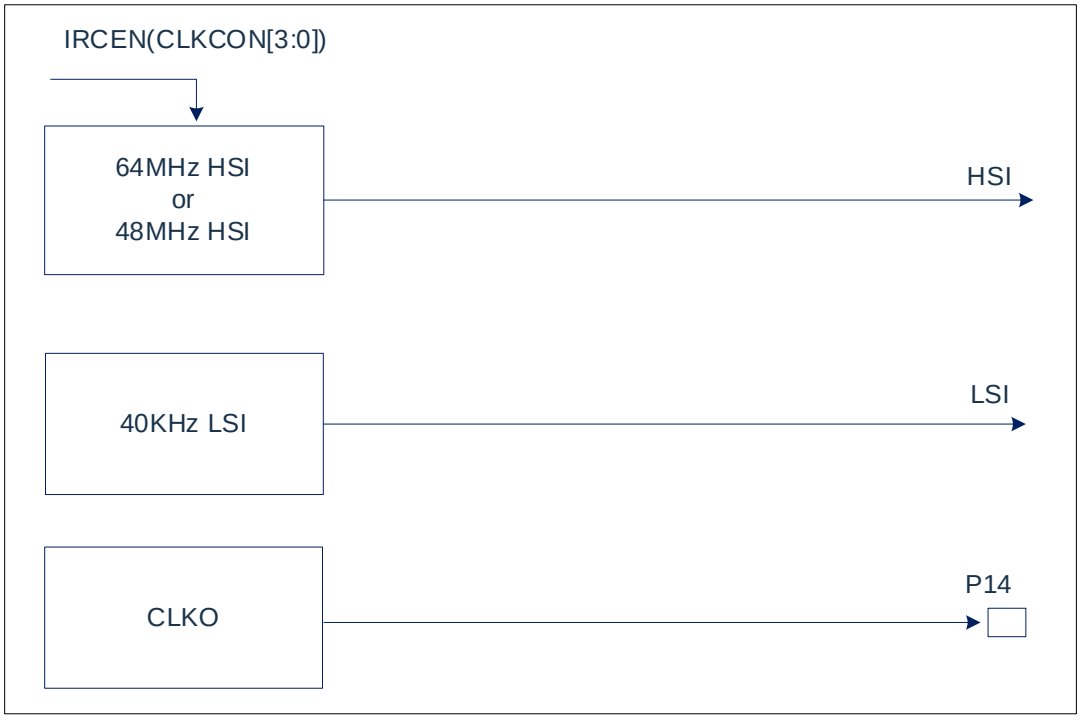


Figure3-1: Block diagram of the clock structure

3.3 Clock control block diagram

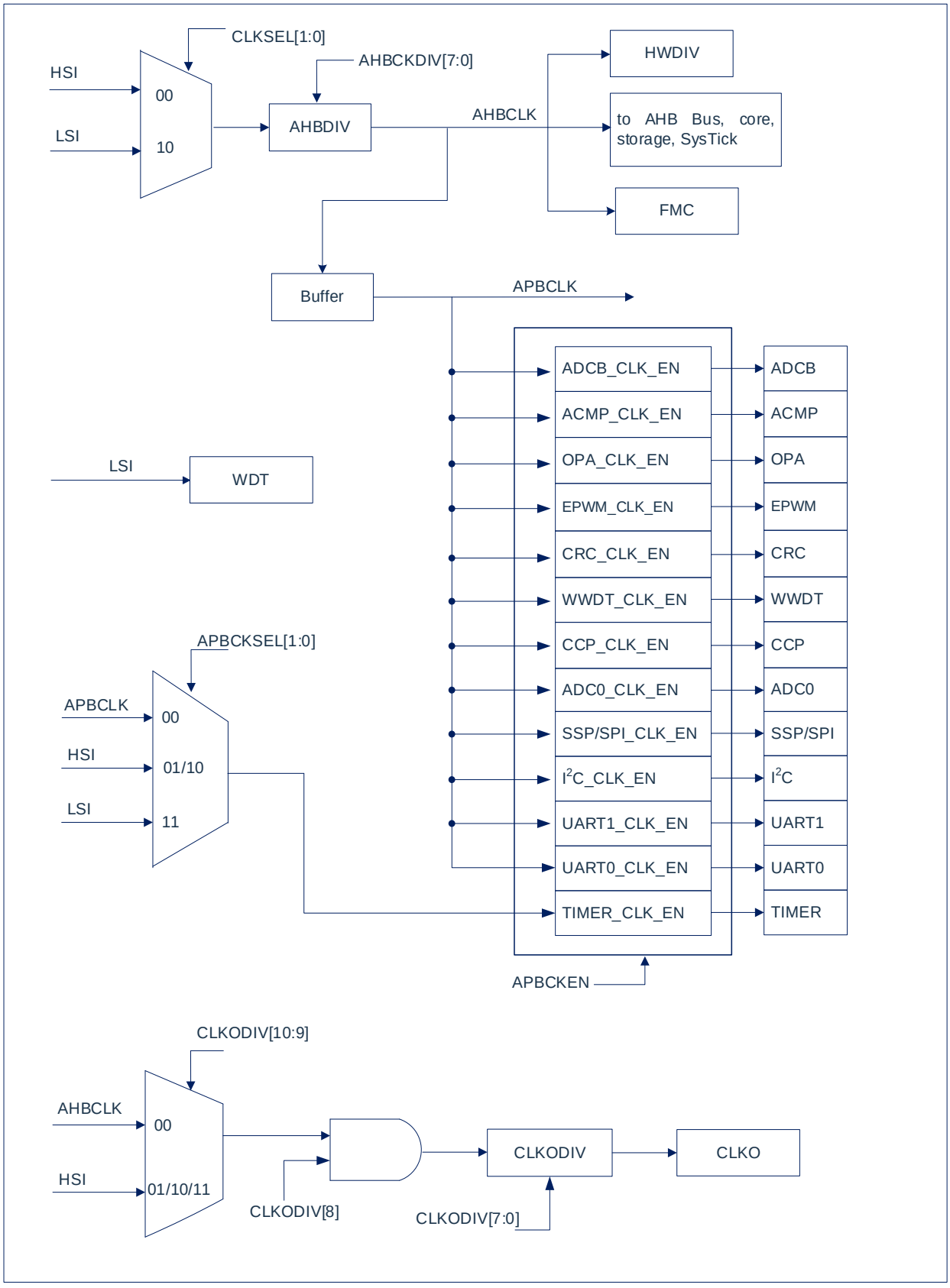


Figure3-2: Clock control block diagram

4. power management

4.1 overview

The chip has different operating modes to adapt to the power consumption requirements of different applications.

4.2 Working mode

The following table lists the available clocks and wake-up sources in different modes.

	Normal mode	Sleep mode (PCON[0]=1)	Deep sleep mode (PCON[1]=1)
definition	The MCU is in normal working condition and the peripherals are running normally and the LDO is turned on	The MCU is asleep, the CPU stops working, and the peripherals are running normally and the LDO is turned on	The MCU is in deep sleep mode, and peripherals other than WDT on the CPU stop working LDODS=0: LDO is enabled LDODS=1: LDO is in a low-power mode
Entry conditions	The chip is in normal mode after the system reset is complete	The sleep mode enable bit is set and the CPU executes the WFI command	The deep sleep mode enable bit is set and the CPU executes the WFI command
Wake up the source	-	All interrupts	I/O interrupt,WDT interrupt
Available clocks	-	All clocks except AHBCLK	Internal low-speed 40KHz clock
Post-wake mode	-	The MCU returns to normal mode and the program continues	The MCU returns to normal mode and the program continues
Wait time after wake-up	-	Run the program immediately	LDODS=0: ~25us@Fsys=48MHz LDODS=1: ~60us@Fsys=48MHz
External reset	Supported (The reset port remains low >100us reset system).	Supported (The reset port remains low >100us reset system).	Supported (The reset port remains low >100us reset system).
Low-voltage reset	Supported	Supported	LDODS=0, supported LDODS=1, not supported
Low voltage detection	Supported	Supported	LDODS=0, supported LDODS=1, not supported
Low power consumption	-	-	LDODS=0: ~200uA LDODS=1: ~5uA

4.3 Power supply low voltage detection (LVD).

The chip contains a low voltage detection circuit that senses the voltage of the chip's supply pin VDD.

The detected voltage point can be set to: 4 2V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V.

5. System Control (SYSCON)

5.1 overview

System control consists of the following sections:

- System reset.
- System power distribution.
- Sleep mode management.
- System management registers for product ID, chip reset, on-chip controller reset, and multifunction pin control.
- System Timer (SysTick).
- Nested interrupt vector controller (NVIC).
- System control registers.

5.2 Register mapping

(SYSCON base address = 0x5000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
DID	0x000	RO	Product ID register	-
AHBCKDIV	0x004	R/W	AHB clock divider register	0x0
APBCKEN	0x00C	R/W	The APB clock enable register	0xFFFFFFFF
CLKODIV	0x010	R/W	Clock output control register	0x0
PCON(P0)	0x014	R/W	Power control register	0x0
RSTCON(P0)	0x018	WO	Reset control register	0x0
RSTSTAT	0x01C	R/W	Reset the status register	-
CLKCON(P0)	0x020	R/W	Clock source control register	0x2F
CLKSEL(P0)	0x024	R/W	Clock source selection register	0x0
CLKSTAT	0x028	RO	Clock source status register	0x1
APBCKSEL	0x02C	R/W	APB clock source selection register	0x0
IOMUX	0x030	RO	IO multiplexed status register	0xFF
CIDL	0x034	RO	UID[63:32]	-
YES	0x038	RO	UID[95:64]	-
LVDCON	0x03C	R/W	LVD control register	0x0
IOP00CFG(P1A)	0x040	R/W	P00 Configuration Register	0x0
IOP01CFG(P1A)	0x044	R/W	P01 Configuration register	0x0
IOP02CFG(P1A)	0x048	R/W	P02 Configuration register	0x0
IOP03CFG(P1A)	0x04C	R/W	P03 Configuration register	0x0
IOP04CFG(P1A)	0x050	R/W	P04 Configuration register	0x0
IOP05CFG(P1A)	0x054	R/W	P05 Configuration register	0x0
IOP06CFG(P1A)	0x058	R/W	P06 Configuration register	0x0
IOP07CFG(P1A)	0x05C	R/W	P07 Configuration register	0x0
IOP10CFG(P1A)	0x060	R/W	P10 Configuration register	0x0
IOP11CFG(P1A)	0x064	R/W	P11 Configuration register	0x0
IOP12CFG(P1A)	0x068	R/W	P12 configuration register	0x0
IOP13CFG(P1A)	0x06C	R/W	P13 configuration register	0x0
IOP14CFG(P1A)	0x070	R/W	P14 Configuration register	0x0
IOP15CFG(P1A)	0x074	R/W	P15 configuration register	0x0
IOP16CFG(P1A)	0x078	R/W	P16 Configuration register	0x0

register	Offset	Read/write	description	Reset value
IOP17CFG(P1A)	0x07C	R/W	P17 configuration register	0x0
IOP20CFG(P1A)	0x080	R/W	P20 configuration register	0x0
IOP21CFG(P1A)	0x084	R/W	P21 configuration register	0x0
IOP22CFG(P1A)	0x088	R/W	P22 configuration register	0x0
IOP23CFG(P1A)	0x08C	R/W	P23 configuration register	0x0
IOP24CFG(P1A)	0x090	R/W	P24 configuration register	0x0
IOP25CFG(P1A)	0x094	R/W	P25 configuration register	0x0
IOP26CFG(P1A)	0x098	R/W	P26 configuration register	0x0
IOP27CFG(P1A)	0x09C	R/W	P27 Configuration register	0x0
IOP30CFG(P1A)	0x0A0	R/W	P30 configuration register	0x0
IOP31CFG(P1A)	0x0A4	R/W	P31 configuration register	0x0
IOP32CFG(P1A)	0x0A8	R/W	P32 configuration register	0x0
IOP33CFG(P1A)	0x0AC	R/W	P33 Configuration register	0x0
IOP34CFG(P1A)	0x0B0	R/W	P34 configuration register	0x0
IOP35CFG(P1A)	0x0B4	R/W	P35 configuration register	0x0
IOP36CFG(P1A)	0x0B8	R/W	P36 configuration register	0x0
IOP37CFG(P1A)	0x0BC	R/W	P37 Configuration register	0x0
IOP40CFG(P1A)	0x0C0	R/W	P40 configuration register	0x0
IOP41CFG(P1A)	0x0C4	R/W	P41 Configuration register	0x0
IOP42CFG(P1A)	0x0C8	R/W	P42 Configuration register	0x0
IOP43CFG(P1A)	CC 0x0	R/W	P43 Configuration register	0x0
IOP44CFG(P1A)	0x0D0	R/W	P44 configuration register	0x0
IOP45CFG(P1A)	0x0D4	R/W	P45 Configuration register	0x0
IOP46CFG(P1A)	0x0D8	R/W	P46 Configuration register	0x0
IOP47CFG(P1A)	0x0DC	R/W	P47 Configuration register	0x0
IOP50CFG(P1A)	0x0E0	R/W	P50 configuration register	0x0
IOP51CFG(P1A)	0x0E4	R/W	P51 Configuration register	0x0
IOP52CFG(P1A)	0x0E8	R/W	P52 configuration register	0x0
IOP53CFG(P1A)	0x0EC	R/W	P53 Configuration register	0x0
IOP54CFG(P1A)	0x0F0	R/W	P54 Configuration register	0x0
IOP55CFG(P1A)	0x0F4	R/W	P55 configuration register	0x0
-	-	-	-	-
SYS_IMSC	0x100	R/W	system detectinterrupt enable register	0x0
SYS_RIS	0x104	RO	system detect interrupt source status register	0x0
SYS_MIS	0x108	RO	system detect enabled interrupt status register	0x0
SYS_ICLR	0x10C	WO	The system detect interrupt clear register	0x0
HSI_TRIM(P0)	0x110	R/W	Internal oscillation frequency trimming register	-
-	-	-	-	-
SRAMLOCK(P0)	0x1B0	R/W	SRAM write-protect register	0x0
GPIO0LOCK	0x1C0	R/W	GPIO0 write enable register	0x0
GPIO1LOCK	0x1C4	R/W	GPIO1 write enable register	0x0
GPIO2LOCK	0x1C8	R/W	GPIO2 write enable register	0x0
GPIO3LOCK	0x1DC	R/W	GPIO3 write enable register	0x0
GPIO4LOCK	0x1D0	R/W	GPIO4 write enable register	0x0
GPIO5LOCK	0x1D4	R/W	GPIO5 write enable register	0x0
IOCFGLOCK	0x1FC	R/W	Port configuration write enable register	0x0

register	Offset	Read/write	description	Reset value
-	-	-	-	-
UIDX	0x500	RO	UID[31:0]	-
PCRCD	0x510	RO	Program checksums	-
UUIDWC0	0x520	CHK	Detect USRID[31:0]	0x0
UUIDWC1	0x524	CHK	Detect USRID[63:32]	0x0
UUIDWC2	0x528	CHK	Detect USRID[95:64]	0x0
UUIDWCS	0x52C	CHK	Detect fixed code	0x0

Note:

1) (P0/P1D) The registers marked are protected registers.
2) (P0): When the marked register writes a valid control bit, it needs to write a fixed value to other bits, otherwise the write operation is invalid, see the register description.
3) (P1A): When IOCFGLOCK==99H, the marked register is allowed to write; = Other values, forbidden to write.

5.3 Register description

5.3.1 Product ID Register (DID)

bit	symbol	description	Reset value
31:16	BOTTOM	Kernel ID	0x4B02
15:0	-	reserved	-

5.3.2 AHB clock divider register (AHBCKDIV)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	AHBDIV	AHB clock division bit 0: HCLK = FSYS 1~255: HCLK = FSYS/(2×DIV)	0x00

5.3.3 APB Clock Enable Register (APBCKEN)

bit	symbol	description	Reset value
31:28	-	reserved	-
27	ADCBCE	ADCB clock enable bit 0: Disable 1: Enable	1
26	ACMPCE	ACMP clock enable bit 0: Disable 1: Enable	1
25	OP/PGACE	OP/PGA clock enable bit 0: Disable 1: Enable	1
24:22	-	reserved	-
21	EPWMCE	EPWM clock enable bit 0: Disable 1: Enable	1
20	CRCCE	CRC clock enable bit 0: Disable 1: Enable	1
19:15	-	reserved	-
14	WWDTCE	WWDT clock enable bit 0: Disable 1: Enable	1
13	-	reserved	-
12	EC SPC	Capture/PWM clock enable bit 0: Disable 1: Enable	1
11	ADC0EC	ADC0 clock enable bit 0: Disable 1: Enable	1
10	-	reserved	-
9	SSP/SPICE	SSP/SPI clock enable bit 0: Disable	1

		1: Enable	
8	-	reserved	1
7	I2CCE	I2C clock enable bit 0: Disable 1: Enable	1
6	TIMER23EC	TIMER23 clock enable bit 0: Disable 1: Enable	1
5	-	reserved	-
4	UART1CE	UART1 clock enable bit 0: Disable 1: Enable	1
3	UART0CE	UART0 clock enable bit 0: Disable 1: Enable	1
2	HWDIVCE	HWDIV clock enable bit 0: Disable 1: Enable	1
1	TIMER01CE	TIMER01 clock enable bit 0: Disable 1: Enable	1
0	WDTCE	WDT clock enable bit 0: Disable 1: Enable	1

5.3.4 Clock output control register (CLKODIV)

bit	symbol	description	Reset value
31:11	-	reserved	-
10:9	CLK_SEL	F_{SEL} clock source select bits 0x0: AHBCLK 0x1: HSI 0x2: HSI 0x3: HSI	0
8	IN	Clock output enable bit 0: Disable CLKO functionality 1: Enable CLKO function	0
7:0	DIV	Clock output divider 0: $F_{CLKO}=F_{SEL}$ 1~255: $F_{CLKO}=F_{SEL}/(2\times DIV)$	0x00

5.3.5 Power Control Register (PCON)

bit	symbol	description	Reset value
31:16	Key	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0000
15:4	-	Must be 0	-
3	LDODS	LDO mode control bit in deep sleep mode (effective when P CON[1]=1). 0: LDO in deep sleep mode is normal working mode 1: LDO in deep sleep mode is a low-power mode	0
2	--	Must be 0	0
1	Deep sleep mode	Deep sleep mode enabled 0: Disable deep sleep mode 1: Deep sleep mode is enabled, and executing WFI instructions will enter deep sleep mode	0
0	Sleep mode	Sleep mode enable bit 0: Disable sleep mode 1: Enable sleep mode, and executing WFI instructions will enter sleep mode	0

5.3.6 Reset Control Register (RSTCON)

bit	symbol	description	Reset value
31:2	RSTKEY	0x156A99A6 needs to be written at the same time to operate on the other bits of this register, and the read value is 0	0x00000000
1	CPURST	Write 1 to reset the Cortex-M0 CPU and FMC module (do not load the boot configuration). Writing 0 does not affect	0
0	MCURST	Write 1 Reset MCU (Reload Boot Configuration) Writing 0 does not affect	0

Note: Write 0x55AA6699 generate MERCUR; Write 0x55AA669A produces CRISP.

5.3.7 Reset Status Register (RSTSTAT)

bit	symbol	description	Reset value
31:3	-	reserved	-
2	CPURS	CPU reset state 0: No CPU reset detected 1: CPU reset detected	-
1	MCURS	MCU reset status 0: No MCU reset is detected 1: MCU reset detected	-
0	WDTRS	WDT reset status 0: No WDT reset is detected 1: WDT reset detected	-

5.3.8 Clock Source Control Register (CLKCON)

bit	symbol	description	Reset value
31:16	Key	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0000
15:4	-	reserved	-
3	IRCEN	Internal high-speed oscillation (HSI) enable bit 0: Disable internal high-speed oscillation 1: Enable internal high-speed oscillation NOTE: The AHB clock source is selected as HSI or when operating Flash, the system automatically enables HSI, independent of this bit.	1
2	-	reserved	-
1:0	IRCSEL	Internal high-speed oscillation (HSI) frequency select bit 0x0: 64MHz 0x1: -- 0x2: -- 0x3: 48MHz Note: When switching different HSI frequencies, it takes about 125us (4 to 5*TLSI) to switch to the selected frequency, during which the CPU is suspended.	0x3

5.3.9 Clock Source Selection Register (CLKSEL)

bit	symbol	description	Reset value
31:16	KEY	The 0x5A69 needs to be written at the same time to operate on the other bits of the register	-
15:2	-	reserved	-
1:0	CLKSEL	AHB clock source select bit 0x0: Internal high-speed oscillation (HSI). 0x1: Write forbidden 0x2: Internal 40KHz low-speed oscillation (LSI). 0x3: Write forbidden Note: Write disable means that the data cannot be written, CLKSEL still selects the previous oscillator	0x0

5.3.10 Clock Source Status Register (CLKSTAT)

bit	symbol	description	Reset value
31:1	-	reserved	-
0	IRCSTB	Internal high-speed oscillation (HSI) status bits 0: Internal high-speed oscillation is prohibited or unstable 1: Internal high-speed oscillation is stable (HSI is selected by default at power-up) Note: (HSI requires a stabilization time of about 4 to 6us from off to on).) The conditions included are: - The AHB clock is switched from LSI to HSI - The low-power mode switches to HSI operating mode - The system waits for the HSI to stabilize before supplying its clock to the core	1

5.3.11 APB Clock Selection Register (APBCKSEL)

bit	symbol	description	Reset value
31:4	-	reserved	-
3:2	TMR23CELLS	Timer 2/3 clock source select bit 0x0: APBCLK 0x1: forbidden 0x2: forbidden 0x3: forbidden	0x0
1:0	TMR01SEL	Timer 0/1 clock source select bit 0x0: APBCLK 0x1: forbidden 0x2: forbidden 0x3: forbidden	0x0

5.3.12 IO Multiplexed Status Register (IOMUX)

bit	symbol	description	Reset value
31:12	-	reserved	-
11:10	RESETPORT	The external reset pin function is read-only 0x0: P07 as an external reset port 0x1: P54 as an external reset port 0x2: External reset prohibits 0x3: External reset prohibits	-
9:0	-	reserved	-

5.3.13 LVD Control Register (LVDCON)

bit	symbol	description	Reset value
31:12	-	Must be 0	0x03
11	TSVEN	The temperature sensor detects the enable bit 0: Disable 1: Enable	0
10	TSVAS	Temperature sensor trim control selection bit 0: Adjusted by factory settings 1: Controlled by TSVADJ	0
9:6	TSVADJ	Temperature sensor trimming (effective when TSVAS=1) When using this adjustment bit, the output of the temperature sensor needs to be adjusted to 1V 0000: 1111:	0x8
5	LVDF	LVD detection flag bit (read-only) 0: The VDD voltage is greater than the set sense voltage (The hardware comes with hysteresis, which is slightly larger than the set detection voltage) 1: The VDD voltage is less than the set sense voltage	0
4	LVDE	LVD detects the enable bit 0: Disable	0

		1: Enable	
3	-	Must be 0	0
2:0	LVDS	LVD sense voltage selection bit 000: 2.0V 001: 2.2V 010: 2.4V 011: 2.7V 100: 3.0V 101: 3.7V 110: 4.0V 111: 4. 2V	0x0

5.3.14 P00 Configuration Register (IOP00CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP00CFG	P00 feature selection 0x0: GPIO 0x1: AN0_9 0x2: TXD1 0x3: SDA 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.15 P01 Configuration Register (IOP01CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP01CFG	P01 feature selection 0x0: GPIO 0x1: AN0_10 0x2: - 0x3: - 0x4: - 0x5: CCP1A 0x6: - 0x7: -	0x0

5.3.16 P02 Configuration Register (IOP02CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP02CFG	P02 feature selection 0x0: GPIO 0x1: AN0_11 0x2: - 0x3: - 0x4: - 0x5: CCP1B 0x6: - 0x7: -	0x0

5.3.17 P03 Configuration Register (IOP03CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP03CFG	P03 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.18 P04 Configuration Register (IOP04CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP04CFG	P04 feature selection 0x0: GPIO/ECAP00 0x1: AN1_0/C0P0 0x2: RXD1 0x3: SCL 0x4: MISO 0x5: - 0x6: - 0x7: -	0x0

5.3.19 P05 Configuration Register (IOP05CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP05CFG	P05 feature selection 0x0: GPIO/ECAP01 0x1: AN1_1/C0P1 0x2: TXD1 0x3: SDA 0x4: MOSI 0x5: - 0x6: - 0x7: -	0x0

5.3.20 P06 Configuration Register (IOP06CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP06CFG	P06 feature selection 0x0: GPIO/ECAP02 0x1: AN1_2/C0P2/A0P1 0x2: - 0x3: - 0x4: NSS 0x5: CCP0A 0x6: - 0x7: -	0x0

5.3.21 P07 Configuration Register (IOP07CFG).

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP07CFG	P07 feature selection 0x0: GPIO 0x1: AN1_3/C0N 0x2: - 0x3: - 0x4: SCLK 0x5: CCP0B 0x6: - 0x7: -	0x0

5.3.22 P10 Configuration Register (IOP10CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP10CFG	P10 feature selection 0x0: GPIO/ECAP03 0x1: AN0_0/C0P3 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: CUSTOM	0x0

5.3.23 P11 configuration register (IOP11CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP11CFG	P11 feature selection 0x0: GPIO 0x1: AN0_1/A1P1 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.24 P12 configuration register (IOP12CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP12CFG	P12 feature selection 0x0: GPIO 0x1: AN0_2/A1GND 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.25 P13 configuration register (IOP13CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP13CFG	P13 feature selection 0x0: GPIO 0x1: TheN1_4/A10 0x2: - 0x3: - 0x4: - 0x5: - 0x6: BKIN 0x7: -	0x0

5.3.26 P14 configuration register (IOP14CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP14CFG	P14 feature selection 0x0: GPIO/ECAP10 0x1: AN1_5/C1P0/A0P0 0x2: - 0x3: SCL 0x4: MISO 0x5: - 0x6: - 0x7: CLKO	0x0

5.3.27 P15 configuration register (IOP15CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP15CFG	P15 feature selection 0x0: GPIO/ECAP11 0x1: AN1_6/C1P1/A0GND 0x2: RXD0 0x3: SDA 0x4: MOSI 0x5: - 0x6: - 0x7: -	0x0

5.3.28 P16 configuration register (IOP16CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP16CFG	P16 feature selection 0x0: GPIO/ECAP12 0x1: AN1_7/C1P2/A0O 0x2: TXD0 0x3: - 0x4: SCLK 0x5: - 0x6: BKIN 0x7: -	0x0

5.3.29 P17 configuration register (IOP17CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP17CFG	P17 feature selection 0x0: GPIO 0x1: AN0_3/C1N/A1P0 0x2: - 0x3: - 0x4: NSS 0x5: - 0x6: - 0x7: SWDDAT0	0x0

5.3.30 P20 configuration register (IOP20CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP20CFG	P20 feature selection 0x0: GPIO/ECAP13 0x1: AN1_8/C1P3 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: SWDCLK0	0x0

5.3.31 P21 configuration register (IOP21CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP21CFG	P21 feature selection 0x0: GPIO 0x1: AN1_9/OP1_O 0x2: CTS0 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.32 P22 configuration register (IOP22CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP22CFG	P22 feature selection 0x0: GPIO 0x1: TheP1_N 0x2: RTS0 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.33 P23 configuration register (IOP23CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP23CFG	P23 feature selection 0x0: GPIO 0x1: TheP1_P 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.34 P24 configuration register (IOP24CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP24CFG	P24 feature selection 0x0: GPIO 0x1: AN1_10 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.35 P25 configuration register (IOP25CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP25CFG	P25 feature selection 0x0: GPIO 0x1: AN1_11/OP0_O 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.36 P26 configuration register (IOP26CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP26CFG	P26 feature selection 0x0: GPIO 0x1: TheP0_N 0x2: - 0x3: - 0x4: - 0x5: CCP1A 0x6: - 0x7: -	0x0

5.3.37 P27 configuration register (IOP27CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP27CFG	P27 feature selection 0x0: GPIO 0x1: AN0_4/OP0_P 0x2: - 0x3: - 0x4: - 0x5: CCP1B 0x6: - 0x7: C1_O	0x0

5.3.38 P30 configuration register (IOP30CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP30CFG	P30 feature selection 0x0: GPIO 0x1: AN0_5 0x2: - 0x3: - 0x4: - 0x5: CCP0A 0x6: - 0x7: C0_O	0x0

5.3.39 P31 configuration register (IOP31CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP31CFG	P31 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: CCP0B 0x6: - 0x7: -	0x0

5.3.40 P32 configuration register (IOP32CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP32CFG	P32 feature selection 0x0: GPIO 0x1: - 0x2: CTS1 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.41 P33 configuration register (IOP33CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP33CFG	P33 feature selection 0x0: GPIO 0x1: - 0x2: RTS1 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.42 P34 configuration register (IOP34CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP34CFG	P34 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.43 P35 configuration register (IOP35CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP35CFG	P35 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.44 P36 configuration register (IOP36CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP36CFG	P36 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.45 P37 configuration register (IOP37CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP37CFG	P37 feature selection 0x0: GPIO 0x1: - 0x2: CTS0 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.46 P40 configuration register (IOP40CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP40CFG	P40 feature selection 0x0: GPIO 0x1: AN0_6 0x2: RTS0 0x3: - 0x4: - 0x5: - 0x6: BKIN 0x7: -	0x0

5.3.47 P41 configuration register (IOP41CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP41CFG	P41 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: BKIN 0x7: -	0x0

5.3.48 P42 configuration register (IOP42CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP42CFG	P42 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: EPWM5 0x7: -	0x0

5.3.49 P43 configuration register (IOP43CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP43CFG	P43 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: EPWM4 0x7: -	0x0

5.3.50 P44 configuration register (IOP44CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP44CFG	P44 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: EPWM3 0x7: -	0x0

5.3.51 P45 configuration register (IOP45CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP45CFG	P45 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: EPWM2 0x7: -	0x0

5.3.52 P46 configuration register (IOP46CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP46CFG	P46 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: EPWM1 0x7: -	0x0

5.3.53 P47 configuration register (IOP47CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP47CFG	P47 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: EPWM0 0x7: -	0x0

5.3.54 P50 configuration register (IOP50CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP50CFG	P50 feature selection 0x0: GPIO 0x1: AVREFN 0x2: RXD0 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.55 P51 configuration register (IOP51CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP51CFG	P51 feature selection 0x0: GPIO 0x1: AVREFP 0x2: TXD0 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.56 P52 Configuration Register (IOP52CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP52CFG	P52 feature selection 0x0: GPIO 0x1: AN0_7 0x2: CTS1 0x3: - 0x4: - 0x5: - 0x6: - 0x7: SWDCLK1	0x0

5.3.57 P53 configuration register (IOP53CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP53CFG	P53 feature selection 0x0: GPIO 0x1: AN0_8 0x2: RTS1 0x3: - 0x4: - 0x5: - 0x6: - 0x7: SWDDAT1	0x0

5.3.58 P54 configuration register (IOP54CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP54CFG	P54 feature selection 0x0: GPIO 0x1: - 0x2: - 0x3: - 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.59 P55 Configuration Register (IOP55CFG)

bit	symbol	description	Reset value
31:3	-	reserved	-
2:0	IOP55CFG	P55 feature selection 0x0: GPIO 0x1: - 0x2: RXD1 0x3: SCL 0x4: - 0x5: - 0x6: - 0x7: -	0x0

5.3.60 System Detection Interrupt Enable Register (SYS_IMSC)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	LVD_IMSC	LVD interrupt enable bit 0: Disable 1: Enable	0
3:0	-	reserved	-

5.3.61 System Detects Interrupt Source Status Registers (SYS_RIS)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	LVD_RIS	LVD interrupt source state 0: The VDD voltage is higher than the set voltage (no interrupts are generated or the interrupts are cleared). 1: The VDD voltage is lower than the set voltage (generating an interrupt).	0
3:0	-	reserved	-

5.3.62 System Detect Enabled Interrupt Status Registers (SYS_MIS)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	LVD_MIS	LVD interrupt status 0: No interrupt was generated 1: Enabled and produced an interrupt	0
3:0	-	reserved	-

5.3.63 System Detect Interrupt Clear Register (SYS_ICLR)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	LVD_ICLR	Write 1 to clear lvd interrupt status Writing 0 does not affect	0
3:0	-	reserved	-

5.3.64 Internal Oscillation Frequency Trimming Register (HSI_TRIM)

bit	symbol	description	Reset value
31:16	-	0x5A69 needs to be written at the same time to operate on the other bits of the register	0
15:8	-	reserved	0
7:0	TRIM	Internal oscillation frequency adjustment bit When powering up or changing the CLKCON[0] bit, the system automatically loads the factory trimming value	-

5.3.65 SRAM write enable register (SRAMLOCK)

bit	symbol	description	Reset value
31:16	LOCK	When LOCK=0x55AA, the protection function of SRAM takes effect	0x0
15:4	-	reserved	-
3:0	REGION	Bit3: Set the SRAM address 0x20001800-0x20001FFF area to a write-protected state Bit2: Set the SRAM address 0x20001000-0x200017FF area to write-protected Bit1: Set the SRAM address 0x20000800-0x20000FFF area to write-protected Bit0: --- Write 0 protection disabled (read/write). Write 1 protection is enabled (read only allowed). Note: The 2KBytes area with an initial address range of 0x20000000-0x2000 07FF is free to read and write.	0x0

5.3.66 GPIO0 Write Enable Register (GPIO0LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the GPIO0 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO0-related registers is prohibited	0x0

5.3.67 GPIO1 write enable register (GPIO1LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the GPIO1 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO1-related registers is prohibited	0x0

5.3.68 GPIO2 write enable register (GPIO2LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the GPIO2 related registers to read the value 0x99 When LOCK= other values, operation ofGPIO2-related registers is prohibited	0x0

5.3.69 GPIO3 write enable register (GPIO3LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the GPIO3-related registers to be read as 0x99 When LOCK= other values, operation of GPIO3-related registers is prohibited	0x0

5.3.70 GPIO4 write enable register (GPIO4LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the operation of the GPIO4 related registers, reading values of 0x99 When LOCK=other values, operation of GPIO4-related registers is prohibited	0x0

5.3.71 GPIO5 write enable register (GPIO5LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the operation of the GPIO5 related registers, reading the value as 0x99 When LOCK= other values, operation of the GPIO 5-related register is prohibited	0x0

5.3.72 The port configuration write enable register (IOCFGLOCK)

bit	symbol	description	Reset value
31:0	IOCFGLOCK	When LOCK=0x99, enables the operation port to configure the associated registers, reading values as 0x99 When LOCK=other values, disable the operation port to configure the associated registers	0x0

6. System Timer (SysTick)

The Cortex-M0® has a built-in system timer, SysTick, which provides a simple 24-bit write clear, decrement counting, auto-loading of initial values, and registers with flexible control mechanisms. The counter can be used as a tick timer for a real-time operating system (RTOS) or as a simple timer peripheral.

When the system timer is enabled, the value of the SysTick current value register (SysTickVAL) is counted down to 0, and at the next clock edge, the value of the SysTick reload value register (SysTickLOAD) is reloaded, and then decremented at any time. When the counter is decremented to 0, the COUNTFLAG status bit is set to 1 and the SysTickCTRL register is read to clear the COUNTFLAG bit.

The clock source for the system timer is the system clock (SCLK).

Note: When the kernel is in a suspended state, the count stops decrementing.

6.1 Register mapping

(SysTick base address = 0xE000_E010) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
SysTickCTRL	0x000	R/W	SysTick control and status register	0x0
SysTickLOAD	0x004	R/W	SysTick reload value register	-
SysTickVAL	0x008	R/W	SysTick current value register	-
SysTickCALIB	0x00C	RO	SysTick calibration value register	0x40028B0A

6.2 Register description

6.2.1 SysTick Control and Status Register (SysTickCTRL)

bit	symbol	description	Reset value
31:17	-	reserved	-
16	COUNTFLAG	When the SysTick counter decrements the count to 0, the bit is set, and reading the register clears it to zero	0
15:3	-	reserved	-
2	-	reserved	-
1	INT	SysTick interrupt enable bit 0: Disable SysTick Interrupt 1: Enable SysTick interrupt	0
0	IN	The SysTick counter enable bit 0: Disable 1: Enable	0

6.2.2 SysTick reload register (SysTickLOAD)

bit	symbol	description	Reset value
31:24	-	reserved	-
23:0	RELOAD	When the counter is enabled and counted to 0, this value reloads the SysTickVAL register.	-

6.2.3 SysTick current value register (SysTickVAL)

bit	symbol	description	Reset value
31:24	-	reserved	-
23:0	CURRENT	The current value of the SysTick counter is returned when the register is read; Write any data to clear the SysTick counter while clearing the COUNTFLAG bit in the SysTickCTRL register.	-

6.2.4 SysTick calibration value register (SysTickCALIB)

bit	symbol	description	Reset value
31	-	reserved	-
30	SKEW	Shows whether the TENS value is accurate, an inaccurate TENS value will affect the match of SysTick as a software real-time clock. 0: The values of TENS are accurate; 1: The value of TENS is inaccurate or does not exist.	0
29:24	-	reserved	-
23:0	TENMS	It is a reloaded value for 10ms timing and is affected by the system clock deviation. If this value is read as 0, the calibration value is indeterminate	0x000004

7. Nested Vector Interrupt Controller (NVIC)

The Cortex-M0® CPU provides a nested vector interrupt controller (NVIC) for interrupt handling.

7.1 characteristic

- Nested vector interrupts are supported.
- Automatically save and restore processor state.
- Dynamically change priorities.
- Simplify and determine interrupt times.

NVIC handles all supported exceptions in priority. All exceptions are handled in "Handler mode". The NVIC supports 32 (IRQ[31:0]) discrete interrupts, each with 4 levels of interrupt priority. All interrupts and most system exceptions can be configured with different priorities. When an interrupt occurs, NVIC will prioritize the new interrupt against the current interrupt, and if the new interrupt has a high priority, the new interrupt will be processed immediately.

When an interrupt is accepted, the start address of the interrupt service program (ISR) is available from the in-memory vector table. The software does not need to decide which interrupt is responded to, nor does it need to assign the start address of the relevant ISR. When the start address is obtained, the NVIC automatically saves the processor status registers (PC, PSR, LR, R0~R3, R12) to the stack. After the ISR ends, the NVIC will recover the values of the relevant registers from the stack and run in a normal state. So it takes a small and certain amount of time to process the interrupt request.

NVIC supports "end-to-end chaining" that can effectively handle back-to-back interrupts, i.e. without saving and restoring the current state, thereby reducing the delay in completing the current ISR to switching to a pending ISR. NVIC also supports "Late Arrival", so it can improve the efficiency of concurrent interrupts. When a higher priority interrupt request occurs before the current ISR starts executing (the stage of saving the processor state and getting the start address), NVIC will immediately process the higher priority interrupt, improving real-time.

For more details, please refer to the ARM®Cortex-M0® Technical Reference Manual and the ARM®v6-M Architecture Reference Manual.

7.2 Exception patterns and system interrupt mapping

The following table lists the exception patterns supported by the series. As with all interrupts, the software can set a level 4 priority for some of these exceptions. The highest user-configurable priority is 0 and the lowest priority is 3. The default priority for all user-configurable interrupts is 0.

Exception name	Exception number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4~10	reserved
SVCall	11	Configurable
Reserved	12~13	reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0~IRQ31)	16~47	Configurable

Note: Priority 0 is the 4th priority in the system, after the three system exceptions of "Reset", "NMI", and "Hard Fault".

7.3 Vector table

Exception number	Interrupt	Vector address	The exception type	description
1-15	-	0x00-0x3c	System exception	
16	0	0x40	GPIO0	P0[7:0] Interrupt
17	1	0x44	GPIO1	P1 [7:0] interrupt
18	2	0x48	GPIO2	P2 [7:0] interrupt
19	3	0x4c	GPIO3	P3 [7:0] interrupt
20	4	0x50	GPIO4	P4 [7:0] interrupt
21	5	0x54	GPIO5	P5 [5:0] Interrupt
22	6	0x58	CCP	Capture/PWM interrupt
23	7	0x5c	ADC0	ADC0 interrupt
24	8	0x60	-	-
25	9	0x64	WWDT	WWDT interrupt
26	10	0x68	EPWM	EPWM interrupt
27	11	0x6c		
28	12	0x70	ADCB	ADCB interrupt
29	13	0x74	ACMP	ACMP interrupt
30	14	0x78	-	
31	15	0x7c	UART0	UART0 interrupt
32	16	0x80	UART1	UART1 interrupt
33	17	0x84	-	
34	18	0x88	-	-
35	19	0x8c	TIMER0	Timer0 interrupt
36	20	0x90	TIMER1	Timer1 interrupt
37	21	0x94	HOURS2	Timer2 interrupt
38	22	0x98	HOURS3	Timer3 interrupt
39	23	0x9c	WDT	Watchdog interrupt
40	24	0xa0	I2C	I2C interrupt
41	25	0xa4	-	-
42	26	0xa8	SSP/SPI	SSP/SPI interrupt
43	27	0xac	-	-
44	28	0xb0	-	-
45	29	0xb4	-	-
46	30	0xb8	-	-
47	31	0xbc	SYS_CHK	System detects interrupt (LVD interrupt).

7.4 Register mapping

(NVIC Base Address = 0xE000_E000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
ISER	0x100	R/W	interrupt setting enable control register	0x0
ICER	0x180	R/W	Interrupt clear enable control register	0x0
ISPR	0x200	R/W	Interrupt setting pending control register	0x0
ICPR	0x280	R/W	Interrupt clear pending control register	0x0
IPR0	0x400	R/W	IRQ0~IRQ3 interrupt priority register	0x0
IPR1	0x404	R/W	IRQ4~IRQ7 interrupt priority register	0x0
IPR2	0x408	R/W	IRQ8~IRQ11 interrupt priority register	0x0
IPR3	0x40C	R/W	IRQ12~IRQ15 interrupt priority register	0x0
IPR4	0x410	R/W	IRQ16~IRQ19 interrupt priority register	0x0
IPR5	0x414	R/W	IRQ20~IRQ23 interrupt priority register	0x0
IPR6	0x418	R/W	IRQ24~IRQ27 interrupt priority register	0x0
IPR7	0x41C	R/W	IRQ28~IRQ31 interrupt priority register	0x0

7.5 Register description

7.5.1 Interrupt set enable control register (ISER)

bit	symbol	description	Reset value
31:0	SEVENTH	Interrupt enable bit Enables one or more interrupts. Each bit represents an interrupt from IRQ0 to IRQ31 (Vector number from 16 to 47). Write operation: 0: invalid 1: Write 1 to enable the related interrupt Read action: 0: The relevant interrupt status is prohibited 1: The relevant interrupt state is enabled NOTE: Reading the register value indicates the current enable state.	0x0

7.5.2 Interrupt Clear Enable Control Register (ICER)z

bit	symbol	description	Reset value
31:0	CLRENA	Interrupt disable bit Disable one or more interrupts. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Write operation: 0: invalid 1: Write 1 to disable related interrupts Read action: 0: The relevant interrupt status is prohibited 1: The relevant interrupt state is enabled NOTE: Reading the register value indicates the current enable state.	0x0

7.5.3 Interrupt set pending Control Register (ISPR)

bit	symbol	description	Reset value
31:0	SETPEND	Sets the interrupt pending bit Write operation: 0: invalid 1: Write 1 to set the pending state. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Read operation: 0: The related interrupt is not in the pending state 1: The related interrupt is in a pending state NOTE: Reading the register value indicates the current pending state.	0x0

7.5.4 Interrupt Clean Pending Control Register (ICPR)

bit	symbol	description	Reset value
31:0	CLRPEND	Clear the interrupt pending bit Write operation: 0: invalid 1: Write 1 to clear the pending state. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Read action: 0: The related interrupt is not in the pending state 1: The related interrupt is in a pending state NOTE: Reading the register value indicates the current pending state.	0x0

7.5.5 IRQ0~IRQ3 interrupt priority register (IPR0)

bit	symbol	description	Reset value
31:30	PRI_3	IRQ3 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_2	IRQ2 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_1	IRQ1 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_0	IRQ0 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.6 IRQ4~IRQ7 interrupt priority register (IPR1)

bit	symbol	description	Reset value
31:30	PRI_7	IRQ7 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_6	IRQ6 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_5	IRQ5 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_4	IRQ4 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.7 IRQ8~IRQ11 interrupt priority register (IPR2)

bit	symbol	description	Reset value
31:30	PRI_11	IRQ11 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_10	IRQ10 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_9	IRQ9 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_8	IRQ8 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.8 IRQ12~IRQ15 interrupt priority register (IPR3)

bit	symbol	description	Reset value
31:30	PRI_15	IRQ15 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_14	IRQ14 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_13	IRQ13 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_12	IRQ12 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.9 IRQ16~IRQ19 Interrupt Priority Register (IPR4)

bit	symbol	description	Reset value
31:30	PRI_19	IRQ19 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_18	IRQ18 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_17	IRQ17 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_16	IRQ16 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.10 IRQ20~IRQ23 interrupt priority register (IPR5)

bit	symbol	description	Reset value
31:30	PRI_23	IRQ23 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_22	IRQ22 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_21	IRQ21 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_20	IRQ20 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.11 IRQ24~IRQ27 interrupt priority register (IPR6)

bit	symbol	description	Reset value
31:30	PRI_27	IRQ27 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_26	IRQ26 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_25	IRQ25 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_24	IRQ24 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

7.5.12 IRQ28~IRQ31 interrupt priority register (IPR7)

bit	symbol	description	Reset value
31:30	PRI_31	IRQ31 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_30	IRQ30 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	reserved	-
15:14	PRI_29	IRQ29 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	reserved	-
7:6	PRI_28	IRQ28 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	reserved	-

8. System Control Module (SCB)

The Status and Operating Mode of the Cortex-M0® are managed by the System Control Module. The associated registers of these system control modules allow the CPUID, Cortex-M0® interrupt priority, and Cortex-M0® power management to be controlled.

For more details, please refer to the "ARM®Cortex-M0® Technical Reference Manual" and the "ARM®v6-M Architecture Reference Manual".

8.1 Register mapping

(SCB base address = 0xE000_ED00). RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
CPUID	0x000	RO	CPUID register	0x410CC200
ICSR	0x004	R/W	Interrupt control status register	0x00000000
AIRCR	0x00C	R/W	Apply interrupt and reset control register	0xFA050000
SCR	0x010	R/W	System control register	0x00000000
SHPR2	0x01C	R/W	System processor priority register 2	0x00000000
SHPR3	0x020	R/W	System processor priority register 3	0x00000000

8.2 Register description

8.2.1 CPUID register (CPUID)

bit	symbol	description	Reset value
31:24	Implementer	Implement the code = 0x41, assigned by ARM	0x41
23:20	Variant	The version number 0x0	0x0
19:16	Constant	Processor architecture = 0xC, which represents the ARMv6-M architecture	0xC
15:4	Partno	Processor product number =0xC20, which stands for Cortex-M0	0xC20
3:0	Revision	Revision number 0x0	0x0

8.2.2 Interrupt Control Status Register (ICSR)

bit	symbol	description	Reset value
31	NMIPENDSET	The NMI set the pending bit Write operation: 0= invalid 1= set the NMI exception as pending Read operation: 0= The NMI exception is not pending 1= NMI exception is pending **Note: Since NMI is the highest priority exception, the processor usually enters NMI exception handling as soon as it detects the bit write 1.** After exception handling is entered, the processor clears out the bit. This means that only when the processor is executing the NMI exception handler, the NMI signal is generated again, and the NMI exception handler reads this bit and returns 1.	0
30:29	-	reserved	-
28	PENDSVSET	PendSV set pending bit Write operation:	0

		0= invalid 1= Set the PendSV exception as pending Read operation: 0= The PendSV exception is not pending 1= PendSV exception is pending **Note: Setting this bit to 1 is the only way to set pending PendSV exceptions.**	
27	PENDSVCLR	PendSV clears the pending bit Write operation: 0= invalid 1= Clears the PendSV exception pending state **Note: This bit is a write-only bit. In order to clear the PENDSV bit, you must write 0 to PENDSVSET and 1 to PENDSVCLR at the same time.**	-
26	PENDSTSET	The SysTick exception set pending bit Write operation: 0= invalid 1= Suspends the SysTick exception Read operation: 0= The SysTick exception is not pending 1= SysTick exception hangs	0
25	PENDSTCLR	SysTick exception clears the pending bit Write operation: 0= invalid 1= Clears the SysTick exception pending state **Note: This bit is read-only. When you want to clear the PENDST bit, you must write 0 to PENDSTSET and 1 to PENDSTCLR at the same time.**	-
24	-	reserved	-
23	ISRPREEMPT	Interrupt preemptive occupied bit If this bit set to 1, a pending exception exits from the debug stop state and enters exception handling. **Note: This bit is read-only**	-
22	ISRPENDING	Interrupt pending flag (excluding NMI and Vaults) 0= The interrupt is not pending 1= Interrupt is pending **Note: This bit is read-only**	0
21	-	reserved	-
20:12	VECTPENDING	The highest priority exception number among pending exceptions 0= There are no exceptions pending Non-0= The highest priority exception number among pending exceptions **Note: These bits are read-only**	0x00
11:9	-	reserved	-
8:0	VECTACTIVE	Contains the current execution exception number 0= Thread mode Non-0= The exception number of the current executing exception **Note: These bits are read-only**	0x00

8.2.3 Apply interrupt and reset control registers (AIRCR)

bit	symbol	description	Reset value
31:16	VECTORKEY	Register access key Write operation: - When writing this register, the VECTORKEY bit field must be set to 0x05FA, otherwise writes will be ignored. - The VECTORKEY bit field is used to prevent the register from being written incorrectly when the system resets or clears the abnormal state. Read operation: The value read out is 0xFA05	0xFA05
15	ENDIANESS	The endianess format of the memory read only 0= Little-endian 1= main aspects	0
14:3	-	reserved	-
2	SYSRESETREQ	System reset request Writing 1 to this bit will cause a reset signal to the chip, indicating that there is a reset request. This bit is a write-only bit, and it is automatically cleared to zero after reset.	0
1	VECTCLRACTIVE	Abnormally valid status clear bit Reserved for debugging use. When writing this register, the user must write 0 to that bit, otherwise unpredictable situations will occur.	0
0	-	reserved	-

8.2.4 System Control Register (SCR)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	SEVONPEND	Sends an event when pending 0= Only enable interrupts or events can wake up the processor, excluding disabled interrupts. 1= Enable events and all interrupts, including disabled interrupts, to wake up the processor. When an event or interrupt enters a pending state, the event signal wakes the processor from the WFE. If the processor is not waiting for an event, the event will be registered and affect the next WFE. Executing SEV instructions or external events also wakes up the processor.	0
3:2	-	Reserved，must be 0	-
1	SLEEPONEXIT	Sleep-On-Exit enabled This bit indicates whether to exit sleep when returning to Thread mode from Handler mode 0= When returned from Thread mode, it does not hibernate 1= When returning to Thread mode from the ISR, go into hibernation or deep hibernation Setting the bit enables an interrupt-driven application, thus avoiding returning to an empty main function application.	0
0	-	reserved	-

8.2.5 System Processor Priority Register 2 (SHPR2)

bit	symbol	description	Reset value
31:30	PRI_11	System Exception Number 11 – Priority of SVCall 0: Highest priority 3: Indicates the lowest priority	0x00
29:0	-	reserved	-

8.2.6 System Processor Priority Register 3 (SHPR3)

bit	symbol	description	Reset value
31:30	PRI_15	System exception number 15 – Priority of SysTick 0: Highest priority 3: Indicates the lowest priority	0x0
29:24	-	reserved	-
23:22	PRI_14	System exception number 14 – Priority of PendSV 0: Highest priority 3: Indicates the lowest priority	0x0
21:0	-	reserved	-

9. General Purpose I/O (GPIO)

9.1 overview

Up to 46 general-purpose I/O pins, each I/O port can be configured by software into a normal input, pull-up input, pull-down input, push-pull output, and no pull-out leakage output mode. These pins can be shared by configuring the chip and other functional pins.

9.2 characteristic

- Five I/O modes.
  - Normal input.
  - Pull-up input.
  - Pull-down input.
  - Push-pull output.
  - Open-drain output without pull-up.
- I/O can be configured to trigger interrupts at edges/levels.
- 2 output current configurations.
- 2-stage I/O speed configuration.

9.3 Feature description

9.3.1 Input mode

Set GPIOxPMS [4n+2:4n] to 000, Px.n pins to input mode, I/O pins to high-impedance state, no drive capability.

9.3.2 Pull-up input mode

Set GPIOxPMS [4n+2:4n] to 001, Px.n pins to pull-up input mode, and I/O pins to internally connect pull-up resistors.

9.3.3 Pull-down input mode

Set GPIOxPMS [4n+2:4n] to 100, Px.n pins to pull-down input mode, and I/O pins to internally connect pull-down resistors.

9.3.4 Push-pull output mode

Set GPIOxPMS [4n+2:4n] to 001, Px.n pins to push-pull output mode, and I/O support digital output function with source/sink current capability. The value of the DO corresponding bit[n] is sent to the corresponding pin.

9.3.5 Open-drain output without pull-up

Set GPIOxPMS [4n+2:4n] to 010, Px.n pins to open-drain output mode, I/O pin digital output function only supports current sinking, and pull resistors are required to drive high. If the DO corresponding bit is '0', the output is low on the pins. If the DO corresponding bit is '1', the pin is set high by an external pull-up resistor.

9.3.6 Interrupt and wake-up capabilities

Each GPIO pin can be set as an interrupt source for the chip. There are five interrupt trigger conditions that can be set: low trigger, high trigger, falling edge trigger, rising edge trigger, and rising and falling edge triggering at the same time. In edge triggering, the user can prevent unexpected interrupt caused by noise by enabling the input signal debounce function.

When the chip enters sleep/deep sleep mode, the GPIO can also wake up the system. The conditions triggered by wake-up are determined by GPIOxIVAL and require the following attention:

The falling edge wakes up, which requires the port level to be raised before entering a low-power state, and the low level after the falling edge requires at least 2 LSI cycles (50us).

The rising edge wakes up, which requires the port level to be pulled low before entering a low-power state, and the high level after the rising edge requires at least 2 LSI cycles (50us).

9.4 Register mapping

GPIO0 base address = 0x5200_0000;

GPIO1 base address = 0x5280_0000;

GPIO2 base address = 0x5300_0000;

GPIO3 base address = 0x5380_0000;

GPIO4 base address = 0x5400_0000;

GPIO5 base address = 0x5480_0000;

RO: read-only; WO: Write only; R/W: Read and write. The x value in the following registers ranges from 0 to 5.

register	Offset	Read/write	description	Reset value
PMS(P1A)	0x000	R/W	GPIOx mode select register	0x0
DOM(P1A)	0x004	R/W	GPIOx data output write mask registers	0x0
DO(P1A)	0x008	R/W	GPIOx data output register	0xff
OF	0x00c	RO	GPIOx pin status data register	-
IMSC(P1A)	0x010	R/W	GPIOx interrupt enable register	0x0
RICE	0x014	RO	GPIOx interrupt source status register	0x0
PUT	0x018	RO	GPIOx enabled interrupt status registers	0x0
ICLR(P1A)	0x01c	WO	GPIOx interrupt state clear register	0x0
ITYPE(P1A)	0x020	R/W	GPIOx interrupt trigger mode register	0x0
IVAL(P1A)	0x024	R/W	GPIOx interrupt trigger value register	0x0
IANY(P1A)	0x028	R/W	GPIOx interrupt edge trigger mode register	0x0
DIDB(P1A)	0x02c	R/W	GPIOx input filtering control register	0x0
DOSET(P1A)	0x030	WO	GPIOx output set register	0x0
DOCLR(P1A)	0x034	WO	GPIOx output clear register	0x0
DR(P1A)	0x038	R/W	GPIOx drive current set register	0xff
SR(P1A)	0x03C	R/W	GPIOx output rate setting register	0xff

Note:

1) (P1A) The registers marked are protected registers.
2) (P1A): When GPIOxLOCK=99H, the marked register is allowed to write; = Other values, forbidden to write.
3) GPIOxLOCK registers are shown in the system control section.

9.5 Register description

9.5.1 GPIOx Mode Selection Register (GPIOxPMS)

bit	symbol	description	Reset value
31	-	reserved	-
30:28	PMS7	Px.7 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0
27	-	reserved	-
26:24	PMS6	Px.6 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0
23	-	reserved	-
22:20	PMS5	Px.5 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0
19	-	reserved	-
18:16	PMS4	Px. 4 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0
15	-	reserved	-
14:12	PMS3	Px. 3 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0
11	-	reserved	-
10:8	PMS2	Px.2 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up	0x0

		0x3: Pull-up input 0x4: Pull-down input Other values: reserved	
7	-	reserved	-
6:4	PMS1	Px.1 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0
3	-	reserved	-
2:0	PMS0	Px.0 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: reserved	0x0

9.5.2 GPIOx data output write mask register (GPIOxDOM)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	HOUSE	Px[7:0] The data output write mask bit 1: DO register This bit of data is not writable 0: DO registers this bit of data is writable	0x0

9.5.3 GPIOx Data Output Register (GPIOxDO)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	DO'S	Px[7:0] output value 1: Output high 0: Output low	0xFF

9.5.4 GPIOx Pin Status Register (GPIOxDI)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	OF	Pin status input data	-

9.5.5 GPIOx interrupt enable register (GPIOxIMSC)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	IMSC[7:0]	Px[7:0] Interrupt enable bit 1: Enable 0: Disable	0

9.5.6 GPIOx interrupt source status register (GPIOxRIS)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	RIS[7:0]	Px[7:0] Interrupt source status bit 1: The pins caused a break 0: The pins are not interrupted	0

9.5.7 GPIOx enabled interrupt status register (GPIOxMIS)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	MIS[7:0]	Px[7:0] Enabled interrupt status bit 1: A pin interrupt is enabled and an interrupt is generated 0: No interrupt was generated	0

9.5.8 GPIOx interrupt state clear register (GPIOxICLR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	ICLR[7:0]	Px[7:0] Interrupt status clear zero bit Write 1 and clear out the corresponding bits of GPIOxRIS and GPIOxMIS	0

9.5.9 GPIOx interrupt trigger mode selection register (GPIOxITYPE)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	ITYPE[7:0]	Px[7:0] Interrupt trigger mode select bit 0: Edge triggering 1: Level triggering	0

9.5.10 GPIOx interrupt trigger value register (GPIOxIVAL)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	IVAL[7:0]	Px[7:0] Interrupt/Sleep Wake Trigger Condition Selection Bit 0: Low-level triggering or falling edge triggering 1: High-level triggering or rising edge triggering	0

9.5.11 GPIOx interrupt edge trigger mode register (GPIOxIANY)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	IANY[7:0]	Px[7:0] Interrupt edge trigger mode select bit 0: The falling or rising edge is triggered, determined by the GPIOxIVAL register 1: Both the rising and falling edges can be triggered	0

9.5.12 GPIOx Input Filter Control Register (GPIOxDIDB)

bit	symbol	description	Reset value
31:11	-	reserved	-
10:8	DBCKS[2:0]	Px input filtering sampling clock selection bits 000: HCLK 001: HCLK/2 010: HCLK/4 011: HCLK/6 100: HCLK/8 101: HCLK/10 110: HCLK/12 111: HCLK/14	0
7:0	DIDB[7:0]	Px[7:0] Input filter enable bit 0: The pin level is detected via the Smit input directly to GPIOxDI and the interrupt edge 1: After the pin level passes through the Smit input, it also needs to be filtered to GPIOxDI and interrupt edge detection Note: The filter circuit consists of a 3-stage DFF and a debounce circuit that filters out positive/negative pulses with input single pulse widths less than two filtered sample clocks. (Filterable pulse width range: 42ns~580ns@Fsys=48MHz)	0

9.5.13 GPIOx output position register (GPIOxDOSET)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	DOS[7:0]	Px[7:0] Output set control bit writes: 0= Does not affect 1= GPIOxDO corresponds to a high bit output (The register is a write-only register and reads as an invalid value)	0x0

9.5.14 GPIOx output clear register (GPIOxDOCLR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	DOC[7:0]	Px[7:0] Output Zero Control Bit Write: 0= Does not affect 1= GPIOxDO corresponds to a low bit output (The register is a write-only register and reads as an invalid value)	0x0

9.5.15 GPIOx Drives Current Set Register (GPIOxDR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	DR[7:0]	Px[7:0] drive current set bit 0= Large drive current 1= Small drive current	0xff

9.5.16 GPIOx output rate setting register (GPIOxSR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	SR[7:0]	Px[7:0] output rate setting bit 0= The output rate is fast 1= The output rate is slow	0xff

10. Watchdog Timer (WDT)

10.1 overview

The watchdog timer is designed to reset the system when it is running to an unknown state. This approach prevents the system from entering an indefinite cycle. In addition, the watchdog timer supports the system wake-up function from sleep/deep sleep mode.

10.2 characteristic

- 32-bit free downward counter.
- WDT_CLK=40KHz.
- Support WDT interrupt and WDT reset function.
- It has WDT register write protection to avoid abnormal operation.

10.3 Feature description

WDT can be set in the user configuration to start after power-on reset of the WDT counter and WDT overflow reset enable (WDTEN=00H after reset), which requires the user configuration bit CONFIG_EN_WDT to be enabled.

After the system reset is complete, WDTLOAD loads the data in the user configuration WDT_TIME, that is, the WDTLOAD default is determined by the WDT_TIME. The WDT overflow time defined by the user can not be defined by the WDT_TIME by modifying the value of the WDTLOAD.

The overflow time is calculated as: $T_{WDTOVER}$=WDTLOAD× count clock period (select the watchdog clock via WDTCON [3:2].).

If the CONFIG_EN_WDT is set to Disabled, the power-on reset of the WDT counter defaults to the stop count state, and there are 2 ways to make the WDT counter start counting after the reset is completed:

1) WDTEN (WDT Reset Enable Control Bit) writes a value that is not equal to 5AH.
2) WDTIEN (WDT Interrupt Enable Control Bit) Write 1.

If the system has a WDT reset, the power-on configuration process is re-performed after the WDT reset, and the reset time is about 4.5ms. After the reset, the WDT count is started and then the WDT reset is started, the time is determined by the WDTLOAD. The interval between the two resets is about 4.5 ms+2×$T_{WDTOVER}$.

After the WDT starts the counter, the 32-bit counter starts at the initial value and counts down, when the count reaches 0, a WDT interrupt is generated, the initial value is automatically loaded, and the downward count is re-counted, and when the second interrupt is generated and the last interrupt flag bit is not cleared, a WDT reset is generated (required).

10.4 Register mapping

(WDT base address = 0x4780_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
CON(P1D)	0x000	R/W	WDT control registers	0x5A00
LOAD(P1D)	0x004	R/W	WDT initial value register	-
VAL	0x008	RO	WDT count value	0xFFFFFFFF
RICE	0x00c	RO	WDT interrupt source status register	0x0
PUT	0x010	RO	WDT enabled interrupt status register	0x0
ICLR(P1D)	0x014	WO	WDT interrupt clear register	-
LOCK	0x500	R/W	WDT write-protect register	0x0

Note:

1) The registers marked (P1D) are protected registers.

2) (P1D): Lock==55AA6699H, the marked register is allowed to write; = Other values, forbidden to write.

10.5 Register description

10.5.1 WDT Control Register (WDTCON)

bit	symbol	description	Reset value
31:17	-	reserved	-
16	DEBUG	DEBUG mode control 0: WDT stop count when the simulation state is paused 1: The WDT count is independent of the simulation state	0
15:8	WDTEN	WDT reset enable 0x5A: Disable WDT reset Other values: Enable WDT reset, when there is no clear interrupt flag after a WDT interrupt occurs, trigger a WDT reset is triggered the next time a WDT interrupt occurs. When enabled reset, whether WDTCON[0] is 1 or not, the WDT interrupt is enabled	0x5A
7:4	-	reserved	-
3:2	WDTPRE	WDT clock selection 0x0: WDT_CLK/1 0x1: WDT_CLK/16 0x2: WDT_CLK/256 0x3: reserved	0
1	-	reserved	-
0	WDTIEN	WDT interrupt enablement 0: Disables WDT Interrupts 1: Enables WDT interrupts	0

10.5.2 WDT Initial Register (WDTLOAD)

bit	symbol	description	Reset value
31:0	WDTLOAD	The WDT counts the initial value. The minimum value is 1	-

10.5.3 WDT count value (WDTVAL)

bit	symbol	description	Reset value
31:0	WDTVAL	The current value of the WDT counter	0xFFFFFFFF

10.5.4 WDT interrupt source status register (WDTRIS)

bit	symbol	description	Reset value
31:1	-	reserved	-
0	WDTRIS	1: Produces a WDT count down overflow interrupt 0: No interrupt was generated	0

10.5.5 WDT enabled interrupt Status Register (WDTMIS)

bit	symbol	description	Reset value
31:1	-	reserved	-
0	WDTMIS	1: Enables a WDT interrupt and produces an interrupt 0: No interrupt was generated	0

10.5.6 WDT Interrupt Clear register (WDTICLR)

bit	symbol	description	Reset value
31:0	WDTICLR	write 0x55AA55AA: Clear the interrupt flag bit and reload the initial value Other values: Does not affect	-

10.5.7 WDT Write Protection Register (WDTLOCK)

bit	symbol	description	Reset value
31:0	WDTREN	write 0x55AA6699: Enables the operation of the WDT-related registers, which read as 0x01 Other values: Disable the operation of WDT-related registers and read as 0x00	0

11. Window Watchdog Timer (WWDT)

11.1 overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specific window time to prevent the program from running into an uncontrollable state under unpredictable conditions.

11.2 characteristic

- The 6-bit down-count value (CNTDAT) and the 6-bit window comparison value (CMPDAT) make the window period more flexible.
- Supports 4-bit value (PSCSEL) selection window watchdog prescale value, and the prescale counter can reach up to 14 bits.

11.3 Feature description

When WWDT is enabled, the 6-bit counter counts down starting from 0x3F, which triggers a WWDT reset:

1) Performs a reload operation when WWDTVAL > CMPDAT.
2) When the WWDTVAL is reduced to 0x00.

WWDT counter from 0x3F count to 0 overflow time: (PSCSEL*1024*64)*T_{APBCLK}.

The reload operation can only be performed when CMPDAT>=WWDTVAL>0 will not cause a WWDT reset. When an interrupt is enabled, WWDTVAL=CMPDAT, an interrupt is generated (it is recommended to perform a reload operation in the interrupt service program before clearing the interrupt flag).

11.4 Register mapping

(WWDT base address = 0x4180_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
WITH	0x000	R/W	WWDT control registers	0x80000000
RL	0x004	WO	WWDT overload register	-
VAL	0x008	RO	WWDT count value	0x3F
RICE	0x00c	RO	WWDT interrupt source status register	0x0
PUT	0x010	RO	The WWDT enabled interrupt status register	0x0
ICLR	0x014	WO	WWDT interrupt clear register	-

11.5 Register description

11.5.1 WWDT Control Register (WWDTCON)

bit	symbol	description	Reset value
31	DEBUG	0: When the simulation state is paused, the WWDT count is not affected 1: When the simulation state is paused, the WWDT count is paused	1
30:22	-	reserved	-
21:16	CMPDAT	Window comparison values	0x00
15:8	-	reserved	-
7:4	PSCSEL	0000: Divide-by-2 0001: Divide-by-4 0010: Divide-by-8 0011: Divide-by-16 0100: Divide by 32 0101: Divide by 64 0110: Divide by 128 0111: Divide by 256 1000: Divide by 512 1001: Divide-by-1024 1010: Divide-by-2048 1011: Divide-by-4096 1100: Divide-by-8192 1101: Divide-by-16384 1110: Divide-by-16384 1111: Divide-by-16384	0x0
3	-	reserved	-
2	WWDTRF	0: No WWDT reset occurred 1: A WWDT reset occurred	0
1	WWDTIEN	WWDT interrupt enable 0: Disables WWDT Interrupt 1: Enables WWDT interrupt	0
0	WWDTEN	WWDT enable 0: WWDT modules are disabled 1: Enables the WWDT module	0

11.5.2 WWDT Overload Register (WWDTRL)

bit	symbol	description	Reset value
31:0	WWDTRL	Write 0x55AA, reload the WWDT count value to 0x3F	-

11.5.3 WWDT count value (WWDTVAL)

bit	symbol	description	Reset value
31:6	-	-	-
5:0	WDTVAL	The current value of the WDT counter	0x3F

11.5.4 WWDT interrupt source status register (WWDTRIS).

bit	symbol	description	Reset value
31:1	-	reserved	-
0	WWDTRIS	1: Generates a WWDT matching interrupt 0: No interrupt was generated	0

11.5.5 WWDT enabled interrupt status register (WWDTMIS).

bit	symbol	description	Reset value
31:1	-	reserved	-
0	WWDTMIS	1: Enables WWDT interrupt and produces an interrupt 0: No interrupt was generated	0

11.5.6 WWDT interrupt clear register (WWDTICLR).

bit	symbol	description	Reset value
31:1	-	reserved	-
0	WDTICLR	Write 1 to clear the interrupt flag bit Other values: Does not affect	-

12. Cyclic redundancy check unit (CRC).

12.1 overview

In order to ensure safety during operation, the IEC61508 standard requires that data be confirmed even during CPU operation. This universal CRC can perform CRC operations as a peripheral function during CPU operation, specifying the data to be confirmed by the program. The universal CRC is not limited to the code flash area and can be used for multi-purpose inspection.

12.2 characteristic

The CRC-generated polynomial uses CRC-16-CCITT's "$X^{16}+X^{12}+X^5+1$".

12.3 Feature description

After writing the CRCIN register, a PCLK clock is needed to save the CRC operation result to the CRCD register. If necessary, you need to read the data of the previous operation before writing, otherwise it will be overwritten by the new operation result.

Here's an example:

Sending data 0x12345678, starting from LSB to MSB to complete.

The order in which it was sent	0001_1110	0110_1010	0010_1100	0100_1000	Sends on a bitwise basis from left to right
	↓	↓	↓	↓	Bitwise in reverse order in bytes
Reverse order results	0111_1000	0101_0110	0011_0100	0001_0010	
CRCIN data	0x78 ->	0x56 ->	0x34 ->	0x12	Enter the data into the CRCIN
	↓				The polynomial is performed 4 times
CRC results	0000_1000_1111_0110				
↓					
CRCD data	0x08F6				hexadecimal

Taking into account the LSB-preferred communication method, the bit order of the input data is first reversed and then calculated. Send data "0x12345678" from LSB, follow "0x78", "0x56" , "0x34", "0x12" in order to write values to the CRCN register, and finally from The CRCD register reads the value as "0x08F6". This is the result of a CRC operation after reversing the bit order of the data "0x12345678".

12.4 Register mapping

(CRC base address = 0x4A00_0000).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
CRCIN	0x000	R/W	CRC input register	0x0
CRCD	0x004	R/W	CRC data registers	0x0

12.5 Register description

12.5.1 CRC Input Register (CRCIN)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	CRCIN	The CRC input requires 8 bits of data to be calculated	0

12.5.2 CRC Data Register (CRCD)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:0	CRCD	The CRC holds the 16-bit result of the operation	0

13. Divider (HWDIV)

13.1 overview

The chip contains a32-bit/32-bit hardware divider.

13.2 characteristic

- Supports division of unsigned/signed numbers.
- Both the quotient and the remainder are 32 bits wide.
- The divide-by-zero flag indicates the bit.
- The fastest operations completion within 6 HCLK clock.
- Writing divisor register initiates division.

13.3 Function description

The divider can select signed mode or unsigned mode through register HWDIVCON[1], and the divider quotient register HWDIVQ and the remainder register HWDIVR can save the complement of the operation result in signed mode HWDIVCON[1]; It is possible to determine whether the divisor is 0 by register HWDIVCON[2], which is a read-only bit; At the same time, the divider can be determined by register HWDIVCON[3], which is a read-only bit, and a read value of 0 indicates that the divider is operating, 1 indicates that the divider is complete, and the bit is also 1 when the divider is idle.

Note that the clock enable bit of the divider is set in register APBCKEN.

13.4 Register mapping

(HWDIV base address = 0x5500_0000).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
CON	0x000	R/W	Divider control registers	0x0
DIVD	0x004	R/W	Divider dividend registers	0x0
DIVS	0x008	R/W	Divider divisor register	0x0
DIVQ	0x00C	RO	Divider operation result quotient	0x0
DIVR	0x010	RO	Remainder of the result of the divider operation	0x0

13.5 Register description

13.5.1 Divider Control Register (HWDIVCON)

bit	symbol	description	Reset value
31:4	-	reserved	-
3	READY	The divider completes the indicator bit 0: Divider operation 1: The divider is complete or in idle	0
2	DIVBY0	Divider divide-zero indicator bit 0: The divisor is not 0 The divisor is 0 1: (The bit is automatically updated after the division operation is completed).	0
1	SIGN	The divider symbol selects the bit 0: Unsigned mode 1: Signed mode	0
0	-	reserved	-

13.5.2 Divider Dividend register (HWDIVD)

bit	symbol	description	Reset value
31:0	DIVIDEND	32 bits are divised	0

13.5.3 Divider divisor register (HWDIVS)

bit	symbol	description	Reset value
31:0	DIVISOR	32-bit divisor	0

13.5.4 Divider quotient register (HWDIVQ)

bit	symbol	description	Reset value
31:0	QUOTIENT	The result quotient of a 32-bit division operation	0

13.5.5 Divider remainder register (HWDIVR)

bit	symbol	description	Reset value
31:0	REMAINDER	The remainder of the result of a 32-bit division operation	0

14. Timer (TIMER0/1/2/3)

14.1 overview

It includes four programmable 32-bit/16-bit counters, namely TIMER0/TIMER1/TIMER2/TIMER3, providing users with convenient timing counting functions.

14.2 characteristic

- Configurable 32-bit/16-bit down counter.
- Each timer has a separate prescaler.
- Provides three counting operation modes: single trigger, cycle counting, and continuous counting.
- Supports chip wake-up from sleep mode.

14.3 Feature description

14.3.1 Single-shot trigger mode

If the timer is operating in single-shot mode, after enabling the timer, the counter loads the initial value from the loading register, counts down, and when the counter is decremented to 0, it stops working and produces an interrupt. To start the single trigger mode again, you need to clear the TMROS bit and then set the TMROS bit.

(When starting the single trigger mode again, it should be noted that when the TMROS bit is cleared, the time to remain 0 must be greater than a timer count period)

14.3.2 Cycle count mode

If the timer works in cycle count mode, after enabling the timer, the counter loads the initial value from the loading register and counts down, and when the counter decreases to 0, the counter loads the initial value from the loading register and continues counting, while producing an interrupt.

14.3.3 Continuous count mode

If the timer works in continuous count mode, after enabling the timer, the counter loads the initial value from the loading register, counting down, and when the counter is decremented to 0, the counter loads the maximum value as the initial value and continues counting while generating an interrupt.

14.3.4 Lazy loading feature

When data is written to the load register, the counter does not continue to decrement, it loads the initial value from the load register on the rising edge of the next TIMER_CLK, and then decrements the count.

When data is written to the lazy load register, the data is written to the load register on the rising edge of the next TIMER_CLK, and if the counter has begun to count, it waits for the current cycle count to be 0 before loading the initial value from the load register.

14.4 Register mapping

(Timer0 base address = 0x4680_0000; Timer1 base address = 0x4680_0100).

(Timer2 base address = 0x4700_0000; Timer3 base address = 0x4700_0100).

RO: read-only; WO: Write only; R/W: read and write;

register	Offset	Read/write	description	Reset value
WITH	0x000	R/W	Timer control register	0x20
LOAD	0x004	R/W	Timer loading register	0x0
VAL	0x008	RO	Timer current value register	0xFFFFFFFF
RICE	0x00c	RO	Timer interrupt source status register	0x0
PUT	0x010	RO	Timer enabled interrupt status register	0x0
ICLR	0x014	WO	Timer interrupts the clear register	-
BGLOAD	0x018	R/W	Timer delay loading register	0x0

14.5 Register description（x=0,1,2,3）

14.5.1 Timer control register (TIMERxCON)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	TMREN	Timer enable bit 0: Disable 1: Enable	0
6	TMRMS	Timer mode select bit 0: Continuous count mode 1: Cycle count mode	0
5	TMRIE	Timer interrupt enable bit 0: Disable interrupt 1: Enable interrupt	1
4	-	reserved	-
3:2	TMRPRE	Timer prescale 00: Divide-by-1 01: Divide-by-16 10: Divide by 256 11: Reserved	0
1	TMRSZ	Timer count bit selection 0: 16-bit counter 1: 32-bit counter	0
0	TMROS	Single trigger mode select bit 0: The mode is determined by the TRMS bit 1: Single-shot trigger mode (Single-shot mode is triggered again, the initial value of which is determined by the TRMS bit)	0

14.5.2 Timer loading register (TIMERxLOAD)

bit	symbol	description	Reset value
31:0	TMRxLOAD	Timer loading registers	0x0

14.5.3 Timer current value register (TIMERxVAL)

bit	symbol	description	Reset value
31:0	TMRxVAL	The timer current count value	0xFFFFFFFF

14.5.4 Timer interrupts the source status register (TIMERxRIS)

bit	symbol	description	Reset value
31:1	-	reserved	-
0	TMRxRIS	The timer interrupts the source state 1: An interrupt is generated 0: No interrupt was generated	0

14.5.5 Timer enabled interrupt status register (TIMERxMIS)

bit	symbol	description	Reset value
31:1	-	reserved	-
0	TMRxMIS	The timer enabled interrupt status bit 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0

14.5.6 Timer interrupt clear register (TIMERxICLR)

bit	symbol	description	Reset value
31:0	TMRxICLR	Write any number, clear the timer interrupt	-

14.5.7 Timer delay loading register (TIMERxBGLOAD)

bit	symbol	description	Reset value
31:0	TMRxBGLOAD	The timer lazy load register (the read value is the value of the last time TMRxLOAD or TIMERxBGLOAD was written).	0x0

15. Capture/Compare/Pulse Width Modulation Module (CCP0/1)

15.1 overview

It contains 2 groups of CCP modules CCP0/CCP1, and each group of CCP corresponds to A and B two channels. CCP0 corresponds to CCP0A/CCP0B, and CCP1 corresponds to CCP1A/CCP1B.

15.2 characteristic

- Up to 2 ccps with up to 4 PWM outputs.
- Each set of CCPs can be set with an independent period.
- CCPn has an internal 16-bit counter that generates a compare/overflow interrupt.
- The CCPn has a stand-alone capture function and can optionally input signals at the A or B pins.
- CCP1 has a 4-channel capture function that can simultaneously capture CCP0A/CCP0B/CCP1A/CCP1B input signals.
- Capture mode 1 supports the reload CCP0 counter function for capture operations.
- The internal channel CAP3 supports analog comparator output capture.
- Internal channel CAP0-CAP3 supports software capture functionality.

15.3 Feature description

15.3.1 Pulse width modulation mode (PWM)

Each set of CCP can output A and B two PWMs: PWMxA, PWMxB, these two channels share a cycle, the output duty cycle can be set independently through CCPDxA, CCPDxB. PWMxA/PWMxB output polarity can be set by PWMxAO/PWMxBOP bits, corresponding to CCPxA/ CCPxB channel output.

When CCPx run bit is set to 1, the 16-bit counter loads the value of the CCPx reload register, counts down, and when the count value is equal to the value of CCP DxA/B, the PWMxA/PWMxB output level changes.

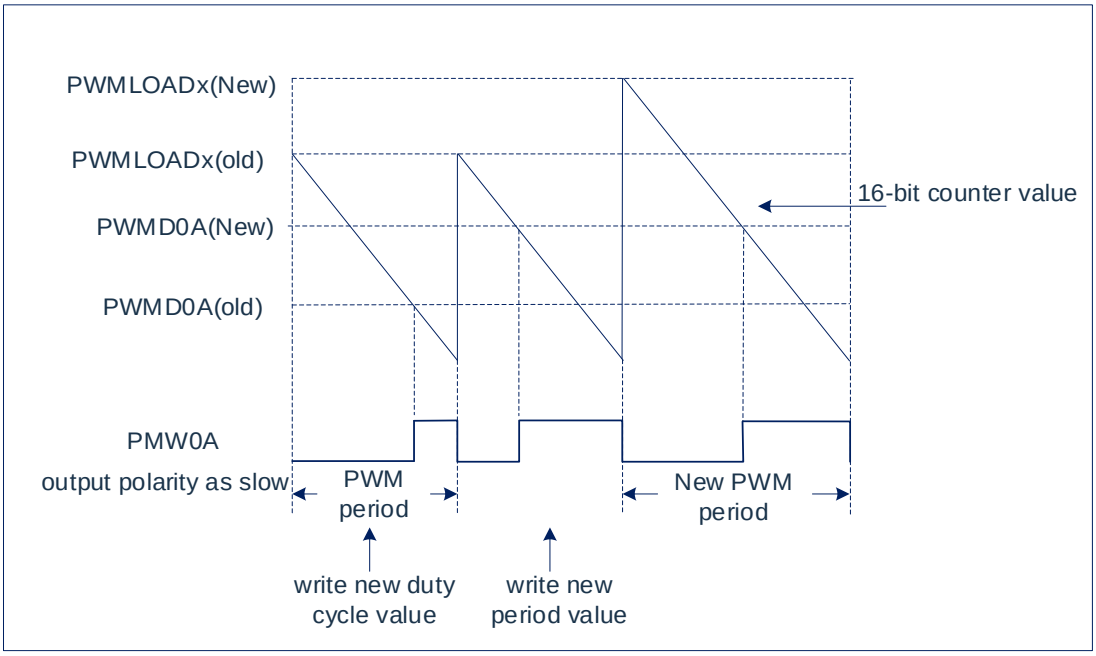


Figure 15-1: PWM timing diagram

Periods and duty cycles are calculated as follows:

Period = CCPLOAD× CCP clock period.

PWMxA duty cycle = CCPDxA/CCPLOADx (supports 0%~100%).

PWMxB duty cycle = CCPDxB/CCPLOADx (supports 0%~100%).

When CCP LOADx=0, PWMxA, PWMxB duty cycle is 0%.

WHEN CCPDxA/CCPDxA> CCPLOADx , the duty cycle is 100%.

15.3.2 Capture mode 0

The capture mode is external capture.

Each set of CCP can be set from A or B as an external capture signal pin, after the CCPRUNx is set, the 16-bit count starts from the 0xFFFF and counts down, when the capture condition is triggered, the counter stops counting, and the CCPxA or CCPxB returns the value of the current counter. If you need to perform the next capture, you need to clear the CCP RUNx and then set it.

The capture time is calculated as follows:

CCPLOADx.RELOAD=0, capture time=(0xFFFF -CCPDxA/B) ×CCPx clock period

CCPLOADx.RELOAD=1, Capture Time=(CCPxLOAD[15:0]-CCPDxA/B) × CCPx clock period

15.3.3 Capture mode 1

CCP1 includes 4 internal channels such as CAP0, CAP1, CAP2, CAP3. One of the channels can be selected as the capture channel either in the external channel ECAP00-03 or ECAP10-13. You can also select CCP0A/CCP0B/CCP1A/CCP1B as the capture channels.

ECAP00-03 corresponds to the positive input C0P0-C0P3 of analog comparator0.

The ECAP10-13 corresponds to the positive input C1P0-C1P3 of analog comparator1.

When using ECAP external capture, the corresponding port needs to be set to GPIO function.

When using CCP0A/CCP0B/CCP1A/CCP1B capture, the corresponding port needs to be set as a CCP port.

Correspondence of CAPn to external channels:

Internal channels	External channels
CAP0	CAP0CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP0CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP0CHS=F: Select CAP0A CAP0CHS = Other values: reserved
CAP1	CAP1CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP1CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP1CHS=F: Select CAP0B CAP1CHS = Other values: reserved
CAP2	CAP2CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP2CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP2CHS=F: Select CAP1A CAP2CHS = Other values: reserved
CAP3	CAP3CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP3CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP3CHS=8: Select the ACMP0 filter to select the output after selection CAP3CHS=9: Select ACMP1 Filter to select the output after selection CAP3CHS=F: Select CAP1B CAP3CHS = Other values: reserved

In Capture Mode 1, PWM mode outputs for CCP0 and CCP1 and External Capture Mode 0 are disabled.

This mode requires CCP1 to operate in count mode, and the capture operation loads the CCP1 count median into the associated registers.

In addition, CCP0 can optionally operate in count mode, and the CAP0-CAP3 capture trigger loading function can be set separately. That is, when the channel is set up to have a capture operation generated, the counter initial value of CCP0 will be reloaded. Multiple channels can set the function at the same time, and software-triggered capture does not reload the initial value of CCP0.

In capture mode 1, the compare/overflow interrupt function of CCP0 andCCP1 can be used normally.

There are two types of capture methods: an external signal trigger capture and a software trigger capture.

1) External signal trigger capture:

   Both cap0-CAP3 can be selected for rising/falling edge or double edge capture. When a signal is generated, the value of the CCP1 counter is captured into the corresponding register and an interrupt flag is generated. The correspondence of the 4 channels to the capture register is as follows:

   CAP0/CAP1/CAP2/CAP3 correspond to cap0DAT/CAP1DAT/CAP2DAT/CAP3DAT registers, respectively.

2) Software triggered capture:

   Write operations to CAP0DAT-CAP3DAT generate capture operations on the CAP0-CAP3 channels. Capture the value of the CCP1 counter to the corresponding register. And the 31-16 bits written must be 0x55AA to trigger the capture operation, which is not related to the low 16 bits of data written. Software-triggered capture does not produce an interrupt flag.

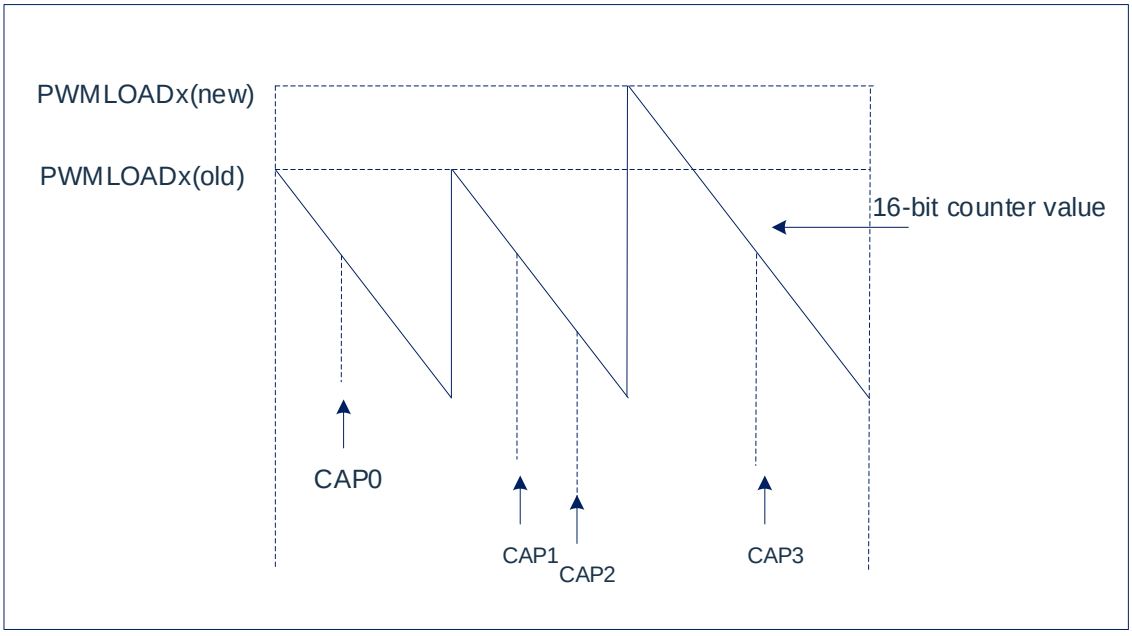


Figure 15-2: CAP0-CAP3 channel capture operation

15.3.4 PWM configuration process

- Configure the PWM control registers, set the prescale, select the PWM mode, and enable PWM.
- Configure the PWM cycle to write to the CCPLOADx registers.
- Configure the PWM duty cycle to write to the CCPDxA/CCPDxB registers.
- If an interrupt is required, enable the associated interrupt bits and clear the interrupt status register.
- Set the corresponding I/O port to the PWM output.
- Set the PWM run register to start the output.

15.3.5 interrupt

In PWM mode, CCPx can generate two types of interrupts:

- When the counter is decremented to 0, an underflow interrupt is generated.
- A comparison interrupt occurs when the value of the counter is equal to the value of CCPDxA or CCPDxB.

At capture mode 0/1, two types of interrupts can be generated:

- When the counter is decremented to 0, an underflow interrupt is generated.
- When a capture condition is triggered, a capture interrupt is generated.

15.4 Register mapping

(CCP base address = 0x4280_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
CCPCON0(P1B)	0x000	R/W	CCP0 control register	0x0
CCPLOAD0(P1A)	0x004	R/W	CCP0 reload register	0x0
CCPD0A(P1A)	0x008	R/W	CCP0 Channel A Data Register	0x0
CCPD0B(P1A)	0x00c	R/W	CCP0 channel B data register	0x0
CCPCON1(P1B)	0x010	R/W	CCP1 control register	0x0
CCPLOAD1(P1A)	0x014	R/W	CCP1 reload register	0x0
CCPD1A(P1A)	0x018	R/W	CCP1 Channel A data register	0x0
CCPD1B(P1A)	0x01C	R/W	CCP1 channel B data register	0x0
-	0x030	-	reserved	-
-	0x034	-	reserved	-
-	0x038	-	reserved	-
-	0x03C	-	reserved	-
CCPIMSC(P1B)	0x040	R/W	CCP interrupt enable register	0x0
CCPRIS	0x044	RO	CCP interrupt source status register	0x0
CCPMIS	0x048	RO	THE CCP enabled interrupt status register	0x0
CCPICLR	0x04C	WO	CCP interrupt clear register	0x0
CCPRUN(P1B)	0x050	R/W	CCP run register	0x0
CCPLOCK	0x054	R/W	CCP0/1 write enable register	0x0
CAPCON(P1B)	0x058	R/W	Capture control register	0x0
CAPCHS(P1B)	0x05C	R/W	Capture channel selection register	0x0
CAP0DAT0(P1A)	0x060	R/W	Capture channel 0 data register	0x0
CAP1DAT0(P1A)	0x064	R/W	Capture channel 1 data register	0x0
CAP2DAT0(P1A)	0x068	R/W	Capture channel 2 data register	0x0
CAP3DAT0(P1A)	0x06C	R/W	Capture channel 3 data register	0x0

Note:

1) (P1A/P1B) The registers marked are protected registers.
2) (P1A): When LOCK==55H or AAH, the marked register is allowed to write; = Other values, forbidden to write.
3) (P1B): When LOCK==55H, the labeled register is allowed to write; = Other values, forbidden to write.

15.5 Register description

15.5.1 CCPx control register (CCPCONx) (x=0,1)

bit	symbol	description	Reset value
31:7	-	reserved	-
6	CCPxEN	CCPx enable bit 0: Disable 1: Enable	0
5:4	CCPxPS	CCPx Prescale selection 0x0: PCLK 0x1: PCLK/4 0x2: PCLK/16 0x3: PCLK/64	0x0
3	CCPxMS	CCPx mode selection 0: Capture mode 0 (effective when CAPEN=0). 1: PWM mode (effective when CAPEN=0).	0
2	CCPxCM0CS	CCPx capture mode 0 capture channel selection 0: Channel CCPxA 1: Channel CCPxB	0
1:0	CCPxCM0ES	CCPx capture mode 0 capture mode selection 0x0: CCPRUNx=1 starts counting, rises along the capture and produces an interrupt 0x1: CCPRUNx=1 starts counting, drops along the capture and produces an interrupt 0x2: The rising edge starts counting, and the falling edge captures and produces an interrupt 0x3: The falling edge starts counting, and the rising edge captures and produces an interrupt	0x0

15.5.2 CCP reload register (CCPLOADx) (x=0,1)

bit	symbol	description	Reset value
31:17	-	reserved	-
16	RELOAD	**CCP0 module:** PWM mode: Reload the enable bit 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP0LOAD Capture mode 0: 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP0LOAD **CCP1 module:** PWM mode: Reload the enable bit 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP1LOAD Capture mode 0, 1: 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP1LOAD	0

15:0	CCPxLOAD	The load value of the CCPx counter (the recommended load value is not 0).	0x0

15.5.3 CCPxA data register (CCPDxA) (x=0,1)

bit	symbol	description	Reset value
31:17	-	reserved	-
16	PWMxAOP	PWMxA output polarity selection 0: Normal output 1: Inverting output	0
15:0	CCPxADATA	In PWM mode: The duty cycle of PWMx A When Capture mode 0: Capture the results	0x0

15.5.4 CCPxB data register (CCPDxB) (x=0,1)

bit	symbol	description	Reset value
31:17	-	reserved	-
16	PWMxBOP	PWMxB output polarity selection 0: Normal output 1: Inverting output	0
15:0	CCPxBDATA	In PWM mode: The duty cycle of PWMx B When Capture mode 0: Capture the results	0x0

15.5.5 CCP Interrupt Enable Register (CCPIMSC)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	CAP3IMSC	CAP3 capture interrupt enable bits 0: Disable 1: Enable	0
10	CAP2IMSC	CAP2 capture interrupt enable bits 0: Disable 1: Enable	0
9	CAP1IMSC	CAP1 capture interrupt enable bits 0: Disable 1: Enable	0
8	CAP0IMSC	CAP0 capture interrupt enable bits 0: Disable 1: Enable	0
7:6	-	reserved	0
5	PWMIMSC	PWM1 overflow interrupt enable bit 0: Disable 1: Enable	0
4	PWMIMSC4	PWM0 overflow interrupt enable bit 0: Disable 1: Enable	0
3:2	-	reserved	-
1	PWMIMSC1	PWM1 compare/capture interrupt enable bits 0: Disable	0

		1: Enable	
0	PWMIMSC0	PWM0 compare/capture interrupt enable bits 0: Disable 1: Enable	0

15.5.6 CCP Interrupt Source Status Register (CCPRIS)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	CAP3RIS	CAP3 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0
10	CAP2RIS	CAP2 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0
9	CAP1RIS	CAP1 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0
8	CAP0RIS	CAP0 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0
7:6	-	reserved	0
5	PWMRIS5	PWM1 overflow interrupt status bit 1: An interrupt is generated 0: No interrupt was generated	0
4	PWMRIS4	PWM0 overflow interrupt status bit 1: An interrupt is generated 0: No interrupt was generated	0
3:2	-	reserved	-
1	PWMRIS1	PWM1 compare/capture interrupt status bit 1: An interrupt is generated 0: No interrupt is generated	0
0	PWMRIS0	PWM0 compare/capture interrupt status bit 1: An interrupt is generated 0: No interrupt is generated	0

15.5.7 CCP enabled interrupt Status Register (CCPMIS)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	CAP3MIS	CAP3 has enabled the capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
10	CAP2MIS	CAP2 has enabled the capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
9	CAP1MIS	CAP1 has enabled capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
8	CAP0MIS	CAP0 has enabled capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
7:6	-	reserved	-
5	PWMMIS5	PWM1 has enabled the overflow interrupt status bit 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
4	PWMMIS4	PWM0 has enabled the overflow interrupt status bit 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
3:2	-	reserved	-
1	PWMMIS1	PWM1 has enabled the Compare/Capture interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0
0	PWMMIS0	PWM0 has enabled the Compare/Capture interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0

15.5.8 CCP Interrupt Clear register (CCPICLR)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	CAP3ICLR	Write 1 to clear the CAP3 capture interrupt status bit	0
10	CAP2ICLR	Write 1 to clear CAP2 capture interrupt status bits	0
9	CAP1ICLR	Write 1 to clear CAP1 to capture interrupt status bits	0
8	CAP0ICLR	Write 1 to clear the CAP0 capture interrupt status bit	0
7:6	-	reserved	-
5	PWMICLR5	Write 1 to clear the PWM1 overflow interrupt status bit	0
4	PWMICLR4	Write 1 to clear the PWM0 overflow interrupt status bit	0
3:2	-	reserved	-
1	PWMICLR1	Write 1 clears the PWM1 compare/capture interrupt status bits	0
0	PWMICLR0	Write 1 to clear the PWM0 compare/capture interrupt status bits	0

15.5.9 CCP Run Register (CCPRUN)

bit	symbol	description	Reset value
31:2	-	reserved	-
1	CCPRUN1	CCP1 operational control bit 0: Stop it 1: run	0
0	CCPRUN0	CCP0 operational control bit 0: Stop it 1: run	0

15.5.10 CCP write enable control register (LOCK)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	LOCK	When LOCK=0xaa, enable to operate the register with protection level of P1A; When LOCK=0x55, enable the operation of registers with protection level P1B and P1A; When LOCK=other values, the operation of registers with protection level is prohibited.	0x0

15.5.11 CAP Control Register (CAPCON)

bit	symbol	description	Reset value
31:13	-	reserved	-
12	CMONKEYS	Capture mode 1 enable bit 0: CCP0/CCP1 is enabled for PWM mode or capture mode 0 1: Capture mode 1 enables, which is full-channel capture mode CCP0 can be set to continuous count mode CCP1 can be set to continuous count mode	0
11	CAP3RLEN	Capture mode 1 CAP3 captures the counter load enable bit that triggers CCP0 0: Disable 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP3 has a capture trigger signal, andCCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0
10	CAP2RLEN	Capture mode 1 CAP2 captures the counter load enable bit that triggers CCP0 0: Disable 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP2 has a capture trigger signal, and CCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0
9	CAP1RLEN	Capture mode 1 CAP1 captures the counter load enable bit that triggers CCP0 0: Disable 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP1 has a capture trigger signal, andCCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0
8	CAP0RLEN	Capture mode 1 CAP0 captures the counter load enable bit that triggers CCP0	0

		0: Disable 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP0 has a capture trigger signal, andCCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	
7:6	CAP3ES	CAP3 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0
5:4	CAP2ES	CAP2 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0
3:2	CAP1ES	CAP1 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0
1:0	CAP0ES	CAP0 capture mode selection 0x0: Disable 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0

15.5.12 CAP Channel Selection Register (CAPCHS)

bit	symbol	description	Reset value
31:17	-	reserved	-
16	ECAPS	ECAP capture channel group selection 0: Choose ECAP00-ECAP03 1: Choose ECAP10-ECAP13	0
15:12	CAP3CHS	CAP3 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0x8: The output of ACMP0 (non-event output). 0x9: The output of ACMP1 (non-event output). 0xF: CCP1B Other values: reserved	0x0
11:8	CAP2CHS	CAP2 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2	0x0

		0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0xF: CCP1A Other values: reserved	
7:4	CAP1CHS	CAP1 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0xF: CCP0B Other values: reserved	0x0
3:0	CAP0CHS	CAP0 captures channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0xF: CCP0A Other values: reserved	0x0

15.5.13 CAP data register (CAPnDAT0) (n=0-3)

bit	symbol	description	Reset value
31:16	-	Read: invalid Write: 0x55aa, a capture operation that produces CAPns Write: Other values are not valid	0x0
15:0	CAPnDATA	Read: Capture the 16bit value of the CCP1 counter for CAPn Write: invalid	0x0

16. Enhanced PWM (EPWM)

16.1 overview

The enhanced PWM module supports six PWM generators and can be configured as 6 independent PWM outputs (EPWM0-EPWM5) or as well 3 pairs of complementary PWMs (EPWM0-EPWM1, EPWM2-EPWM3, EPWM4-EPWM5) with programmable dead-zone generators, respectively.

Each pair of PWMs shares an 8-bit prescaler with 6 clock dividers that provide 5 divider factors (1, 1/2, 1/4). 、1/8、1/16）. Each PWM output is controlled by a separate 16-bit counter, and a 16-bit comparator is used to adjust the duty cycle. The 6-channel PWM generator provides 28 interrupt flags, and the period or duty cycle of the relevant PWM channel matches the counter and will produce interrupt flags for each PWM There are separate enable bits.

Each PWM can be configured as a single mode (which generates a PWM signal period) or a cyclic mode (continuous output of the PWM waveform).

16.2 characteristic

The Enhanced PWM Module has the following features:

- 6 independent 16-bit PWM control modes.
  - 6 independent outputs: EPWM0, EPWM1, EPWM2, EPWM3, EPWM4, EPWM5;
  - 3 complementary PWM pairs: (EPWM0-EPWM1), (EPWM2-EPWM3), (EPWM4-EPWM5), programmable dead-zone can be inserted;
  - 3 sets of synchronous PWM pairs: (EPWM0-EPWM1), (EPWM2-EPWM3), (EPWM4-EPWM5), each set of PWM pairs pin synchronization.
- Support group control, EPWM0, EPWM2, EPWM4 output synchronization, EPWM1, EPWM3, EPWM5 output synchronization.
- Single-shot mode (edge alignment only) or auto-load mode.
- Support edge alignment, center alignment 2 modes.
- Center alignment mode supports symmetric and asymmetric counts.
- Programmable dead-zone generators are supported in complementary PWMs.
- Each PWM has independent polarity control.
- Fault brake protection and recovery functions (hardware/software triggering and hardware/software recovery).
- The ADC comparison event triggers hardware brake protection.
- The ACMP analog comparator triggers hardware brake protection
- The PWM edge or period can trigger the initiation of the AD conversion.

16.3 Feature description

Description of the relevant name:

1) Periodic point: When the counter CNTn is counted to equal to the periodic PERIODn, it is called the periodic point. The resulting interrupt is PIFn
2) Zero point: When the counter CNTn counts to 0, it is called the zero point. The resulting interrupt is ZIFn
3) Up-compare point: When the counter CNTn is counted to equal to CMPDATn, it is called the up-compare point. The resulting interrupt is UIFn. Edge alignment counts have no up-compare points.
4) Down compare point: When the counter CNTn is subtracted to equal to CMPDATn or CMPDDATn, it is called a down compare point. The resulting interrupt is DIFn
5) Midpoint: The midpoint is the middle point, the middle point is the center of the alignment counting mode when the CNTn counts to the moment equal to the CMPDATn or CMPDDATn, because the CNTn will be reduced to 0 after that, so the moment is called the midpoint, Also for the periodic point. Edge alignment count has no midpoint, but has a periodic point.

Note:

1) When the edges are aligned, the period data is loaded at the beginning of the first count, which will produce a period point; At other moments, after the counter counts to 0, the period data needs to be loaded immediately. So the subsequent period point is the same as the position of the zero point. There is a down comparison point for this alignment, not an up comparison point.
2) When the center is aligned, the first count starts counting upwards from 0 and results in a zero point. When the period data is counted, a period point (midpoint) is generated. The zero point alternates with the midpoint. The alignment has an upward comparison point and a downward comparison point, and when the symmetry is counted, the upward comparison point and the downward comparison point are determined by CMPDATn; For asymmetric counting, the upward comparison point is determined by CMPDATn and the downward comparison point is determined by CMDDATn.

16.3.1 Block diagram

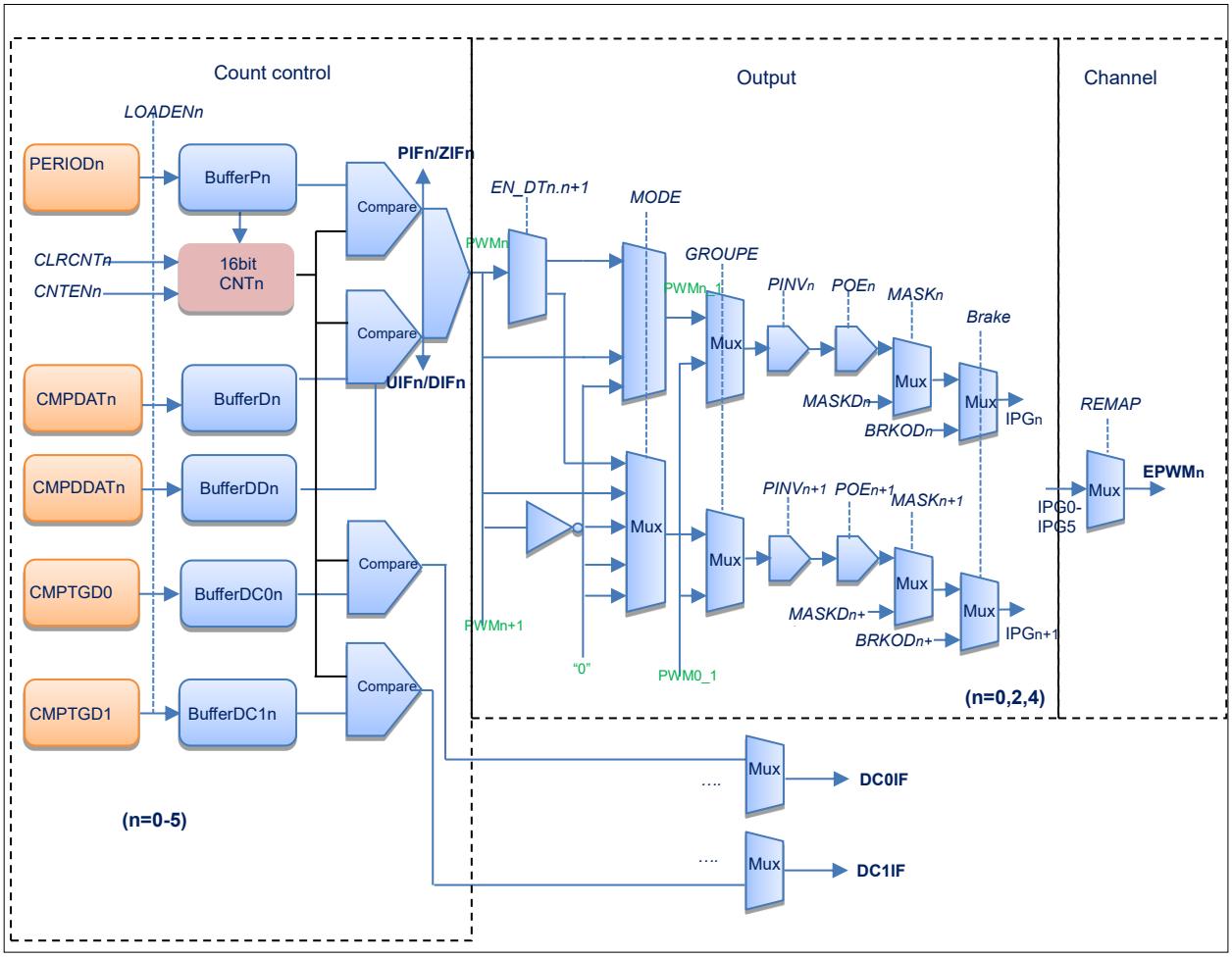


Figure 16-1: The signal of IPGn is the signal before the EPWMn remapping.

16.3.2 Clock divider

Each pair of PWMs shares an 8-bit prescaler, and after the prescale, each PWM can choose (1, 1/2, 1/4, 1/8, 1/16) 5 divider ratios.

PWM_CLK = PCLK / (CLKPSCxx + 1) / CLKDIVn, where xx can be 01, 23, 45, n=0-5.

16.3.3 Independent output mode

The six EPWM channel outputs do not affect each other and operate according to their respective period/duty cycle data

16.3.4 Complementary output modes

In complementary output mode, the 6 PWMs are divided into 3 pairs, EPWM0 and EPWM1 are 1 pair, EPWM2 Paired 1 with EPWM3 and 1 pair with EPWM5. There are 3 pairs of PWM in total.

EPWM0-EPWM1 operates on epwm0's period/duty cycle data, and EPWM0 is inverted from the EPWM1 waveform.

EPWM2-EPWM3 operates on epwm2's period/duty cycle data, and EPWM2 is inverted from the EPWM3 waveform.

EPWM4-EPWM5 operates on epwm4's period/duty cycle data, and EPWM4 is inverted from the EPWM5 waveform.

In this mode, the EPWM1/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

Dead-zone delay control is supported in complementary mode.

16.3.5 Synchronous output mode

In synchronous output mode, the 6 PWMs are divided into 3 pairs, EPWM0 and EPWM1 are 1 pair, EPWM2 Paired 1 with EPWM3 and 1 pair with EPWM5. There are 3 pairs of PWM in total.

EPWM0-EPWM1 operates on the period/duty cycle data of EPWM0, which is in phase with EPWM1 waveform.

EPWM2-EPWM3 operates on the period/duty cycle data of EPWM2, which is in phase with EPWM3 waveform

EPWM4-EPWM5 operates on the period/duty cycle data of EPWM4, which is in phase with EPWM5 waveforms.

In this mode, the EPWM1/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

16.3.6 Grouped output mode

GROUPEN=1 enables the group function, 6 channels of PWM are divided into 2 groups, EPWM0, EPWM2, EPWM4 Group 1, EPWM1, EPWM3, EPWM5 is group 1.

EPWM0-EPWM2-EPWM4 operates on EPWM0's period/duty cycle data, with 3 channels in phase.

EPWM1-EPWM3-EPWM5 operates on EPWM1 period/duty cycle data, with 3 channels in phase.

When the grouping function is turned on, the EPWM2/EPWM4/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

16.3.7 Load update mode

There are two counter loading modes: one-shot mode and continuous mode (auto loading mode).

Single-shot mode:

The period duty cycle relevant data is loaded once at the beginning of the counter, and the output PWM period is related to the loading mode.

LoadTYPn=0, edge alignment is 1 period and center alignment is 0.5 periods.

When LOADTYPn=1, edge alignment is 2 periods and center alignment is 1 period.

LoadTYPn=2, edge alignment is 3 periods and center alignment is 1.5 periods.

At LOADTYPn=3, the edge alignment is 4 periods and the center alignment is 2 periods.

Continuous mode:

The period duty cycle data is automatically loaded at the zero and midpoints of the PWM period. Midpoint loading exists only in center alignment count mode.

In edge alignment counting mode, a zero point is generated at the same time as a periodic point, and the count comparison circuit reloads the value of CMPDATn/PERIODn/CMPTGD0/CMPTGD1.

In center-align count mode, both the midpoint and the zero point are automatically loaded with values for the associated registers. Such a structure supports the first half waveform period duty cycle and the second half waveform period duty cycle.

Due to the dual cache structure of EPWM, during EPWM operation, the value of the relevant operating registers: CMPDATn/CMPDDATn/PERIODn/CMPTGD0/CMPTGD1 is changed, and the PWM output waveform does not change immediately. The values of these registers are loaded into the corresponding cache only at the zero or periodic point.

Such a structure does not immediately change the output waveform in the current PWM period or half-period after changing the period duty cycle data, and the PWM waveform will not change accordingly in the next period or half-period. That is, any changes in PWM-related data do not affect the current full PWM period or half-period.

In high-speed applications, it is possible that the load point has arrived, but the operation of writing to the operating register has not yet been completed. At this point, you do not expect some of the running data to have been loaded and another part of the running data to be unloaded.

For this high-speed application. The EPWM module provides a loading enable bit, after changing the relevant operating register, you need to set the load enable bit LOADENn to 1, and the LOADENn bit is automatically cleared after loading. This bit can also be read to determine whether the value of the associated register is loaded into the actual circuit. If LOADENn= 0, it means that it has been loaded, which will affect the PWM waveform being output; If LOADENn=1, it means that the current PWM waveform has not yet changed, and the value of the register that changed before the next load point will be loaded. If you change the value of the associated run register again, you also need to reset loadENn to 1.

By default, PWM loads the operating data of the relevant registers at both the zero and periodic points, and generates zero and periodic interrupts. In order to adapt to more flexible application requirements. PWM supports different loading modes and zero/periodic point interrupt generation.

In register EPWMCON3 LOADTYPn(0-5) can be set to load mode and zero/period point interrupt mode:

LOADTYEn	Center alignment loading	Edge alignment loading
00	Each zero and periodic point is loaded with and produces zero and periodic interrupt flags	Each zero or periodic point is loaded with zero and periodic interrupt flags
01	Each zero point is loaded with a zero interrupt flag	Every 2 zeros are loaded with a zero interrupt flag
10	The first zero point is loaded alternately with the next period point, resulting in a zero and period point interrupt flag	Every 3 zeros or period points are loaded with a zero and periodic interrupt flag
11	Every two zeros are loaded with a related zero interrupt flag	Every 4 zeros are loaded with a zero interrupt flag

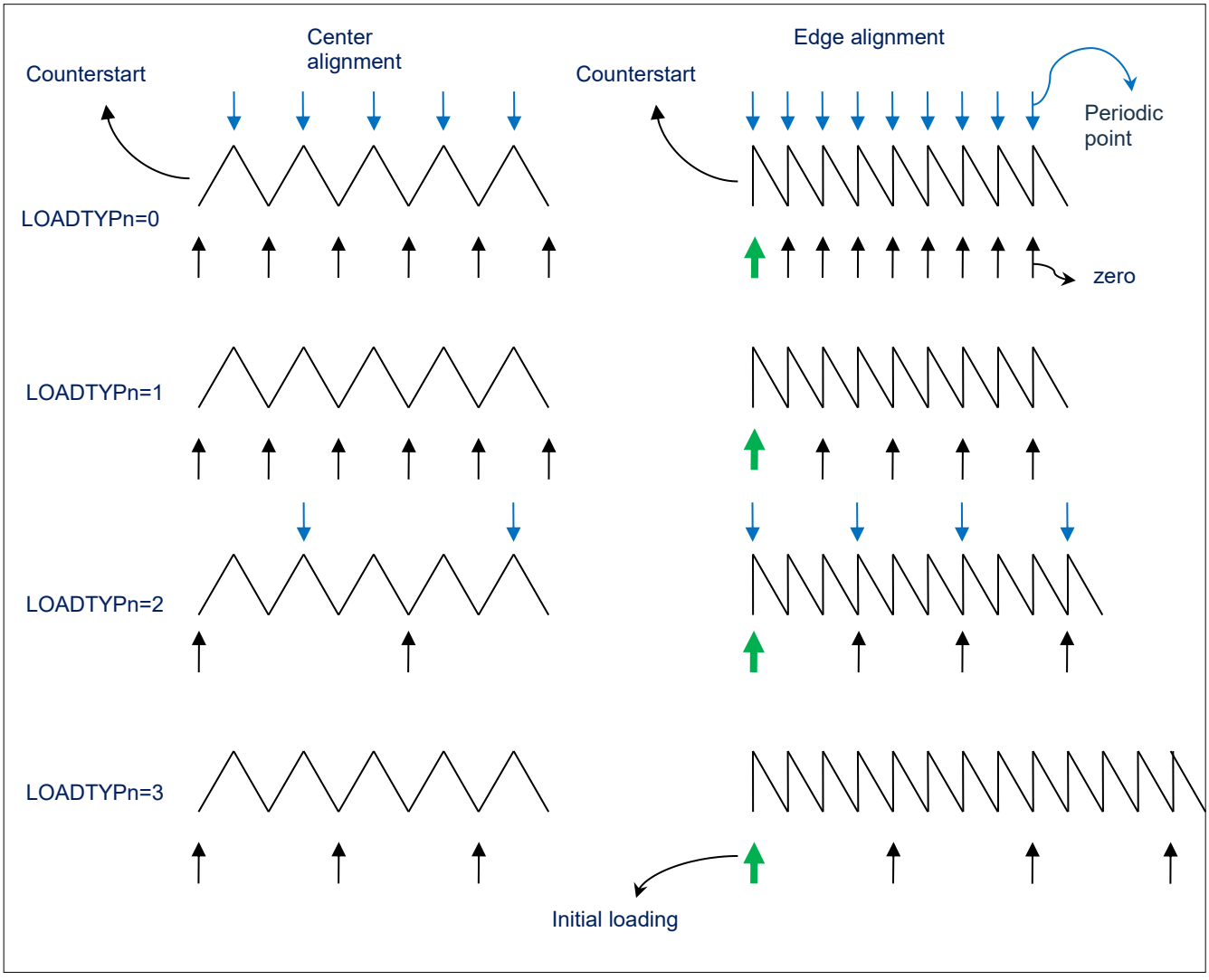


Figure 16-2: PWM period/duty cycle loading update block diagram

16.3.8 Edge alignment count mode

In edge alignment mode, the counting method is down, that is, minus 1 count. The 16-bit PWM counter CNTn counts down at the beginning of each period, compared to the latched CMPDATn value when CNTn=CMPDATn EPWMn Output high, CMPnDIF set to 1. THE CNTn continues to count down to 0, at which point EPWMn will output low, and the current CMPDATn and PERIODn are at The case of PWMnCNTM=1 is reloaded and the PIF period interrupt flag is set.

The relevant parameters for edge alignment are as follows:

$$\text{High Voltage Duration} = (\text{CMPDATn}+1) \times \text{Tpwm}$$

$$\text{Period} = (\text{PERIODn}+1) \times \text{Tpwm}$$

$$\text{duty cycle} = \frac{\text{CMPDATn}+1}{\text{PERIODn}+1}$$

If CMPDATn > PERIODn, the duty cycle is 100%, and the EPWMn channel is always high. And there is no down-to-compare interrupt.

If CMPDATn=0, the duty cycle is 0%.

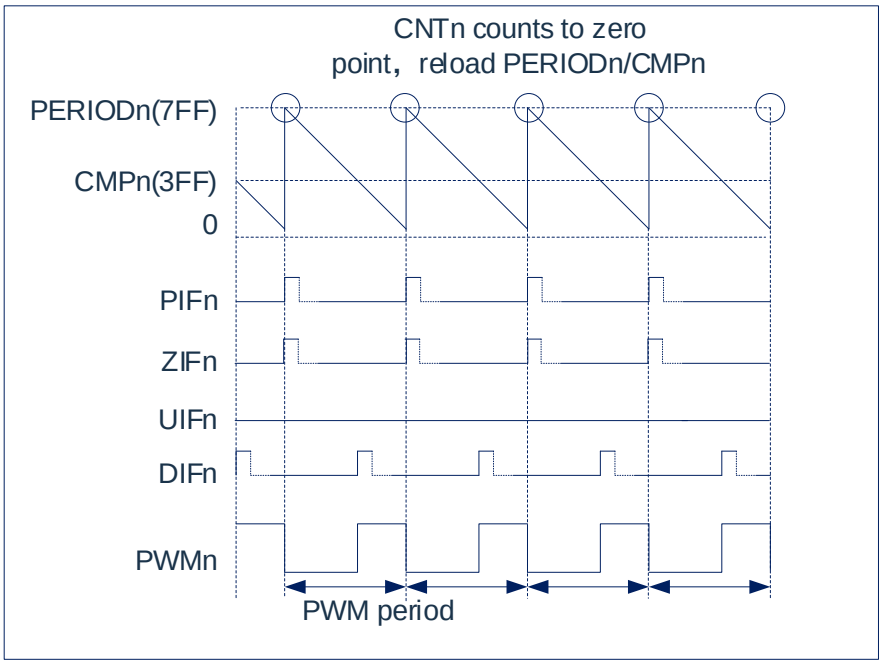


Figure 16-3: Edge alignment mode waveform plot

16.3.9 Center alignment count mode

In center-align mode, the counting method is counting up and then counting down.

The center alignment mode is divided into two symmetrical ways: symmetrical counting mode and asymmetric counting mode.

The symmetric count mode (ASYMEN=0) duty cycle is determined by CMPDATAn.

The asymmetric count mode (ASYMEN=1) duty cycle is determined by CMPDATAn and CMPDDATn.

In the center-aligned symmetrical counting mode, the 16-bit PWM counter CNTn counts upwards from 0, and when CNTn=CMPDATn, the EPWMn output is high. CnTn then continues to count upwards to equal to PERIODn, then CNTn begins to count downwards, and in the process of counting down CNTn = CMPDATn, EPWMn Outputs a low level, after which it continues to count down to 0.

$$High\ Voltage\ Duration = (PERIODn \times 2 - CMPDATn \times 2 - 1) \times Tpwm$$

$$Period = (PERIODn) \times 2 \times Tpwm$$

$$Duty\ Cycle = \frac{PERIODn \times 2 - CMPDATn \times 2 - 1}{PERIODn \times 2}$$

If CMPDATn > = PERIODn, the duty cycle is 0%, the EPWMn channel is always low, and there is no upward comparison interrupt and downward comparison interrupt.

If PERIODn=0, the duty cycle is 0%, the EPWMn channel is always low, and the zero-point interrupt and the periodic point interrupt are always present when CNTn is enabled.

If CMPDATn=0, the duty cycle is 100%.

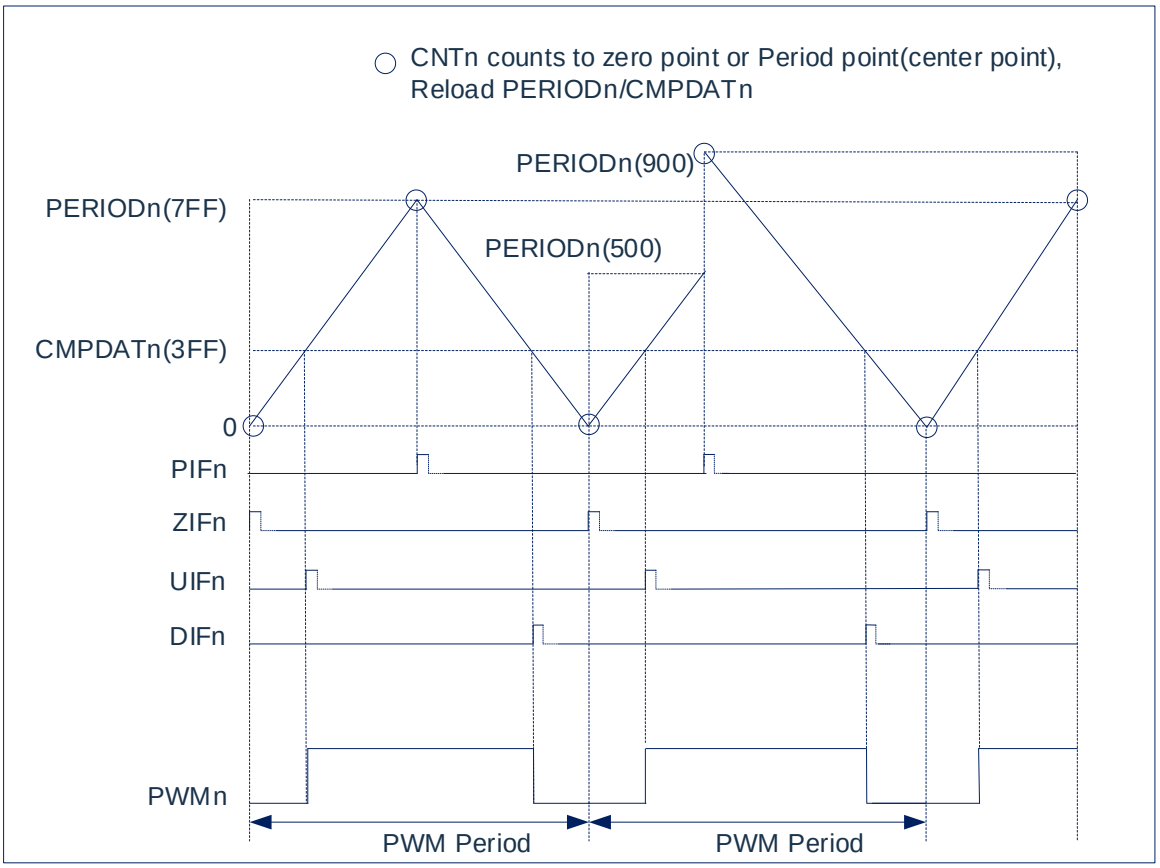


Figure 16-4: Center alignment mode symmetrical counting waveform plot

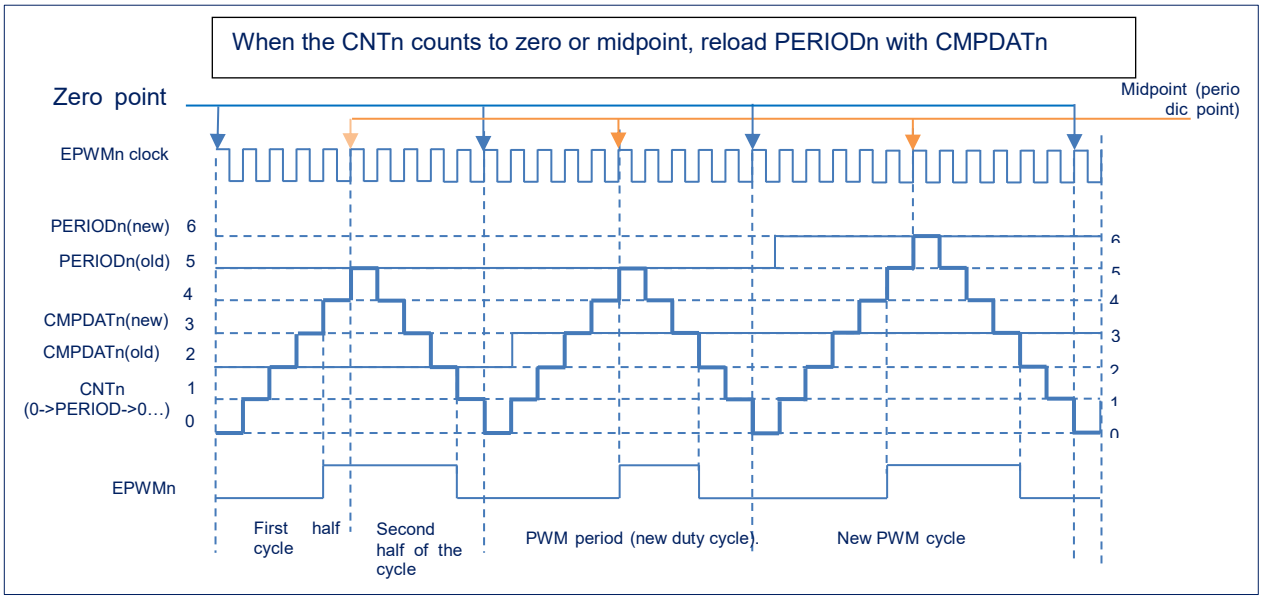


Figure 16-5: Center-aligned counter waveform (symmetrical count).

In the center-aligned asymmetric counting mode, the 16-bit PWM counter CNTn counts upwards from 0, and when CNTn= CMPDATn, the EPWMn output is high , after which cnTn continues to count upwards to equal to PERIODn, then CNTn begins to count downwards, and in the process of counting down CNTn = CMPDDATn, EPWMn Outputs a low level, after which it continues to count down to 0. To enable the asymmetric counting method, the ASYMEN needs to be placed at 1, and the asymmetric counting method can achieve accurate center alignment waveforms.

The relevant parameters for the center-aligned asymmetric count are as follows:

High voltage duration =（PERIODn×2-CMPDDATn-CMPDATn-1）×Tpwm

Period =（PERIODn）×2×Tpwm

$$duty\ cycle = \frac{PERIODn\times2-CMPDDATn-CMPDATn-1}{PERIODn\times2},\quad (CMPDATAn<PERIODn, CMPDDATn<PERIODn)$$

$$duty\ cycle = \frac{PERIODn-CMPDDATn-1}{PERIODn\times2},\quad (CMPDATAn\geq PERIODn, CMPDDATn<PERIODn)$$

$$duty\ cycle = \frac{PERIODn-CMPDATn}{PERIODn\times2},\quad (CMPDATAn<PERIODn, CMPDDATn\geq PERIODn)$$

duty cycle =0%,（CMPDATAn≥PERIODn,CMPDDATn≥PERIODn）

CMPDATAn does not produce an upward comparison interrupt when >=PERIODn.

CMPDDATAn does not produce a downward comparison interrupt when >=PERIODn.

If PERIODn=0, the duty cycle is 0%, the EPWMn channel is always low, and the zero-point interrupt and the periodic point interrupt are always present when CNTn is enabled.

If CMPDATn=0 and CMDATDn=0, the duty cycle is 100%.

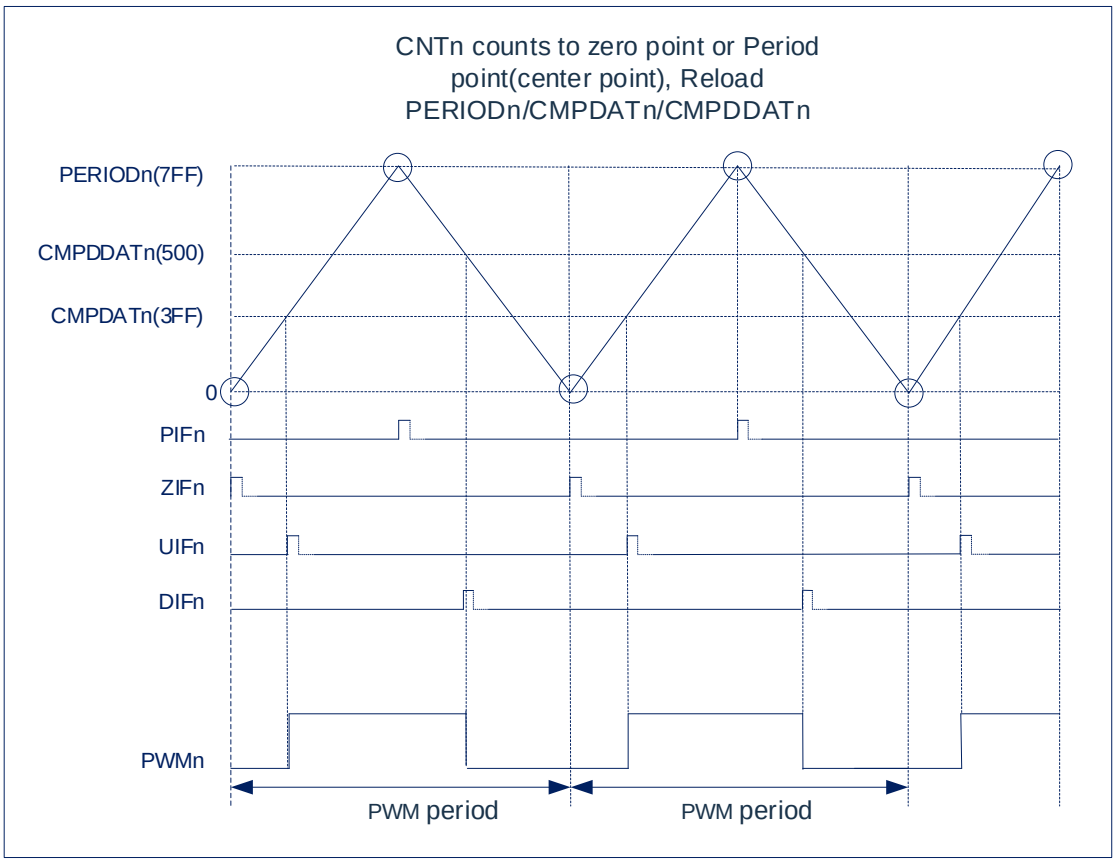


Figure 16-6: Asymmetric count waveform plot in center alignment mode

16.3.10 Independent counter comparison function

During the PWMn Channel Counter (CNTn) counter, two digital comparators are provided, and the counter CNTn is compared to the preset value, and if the counter value is equal to the preset value, an interrupt signal or an ADC operation can be triggered. This feature does not affect the output of the PWM.

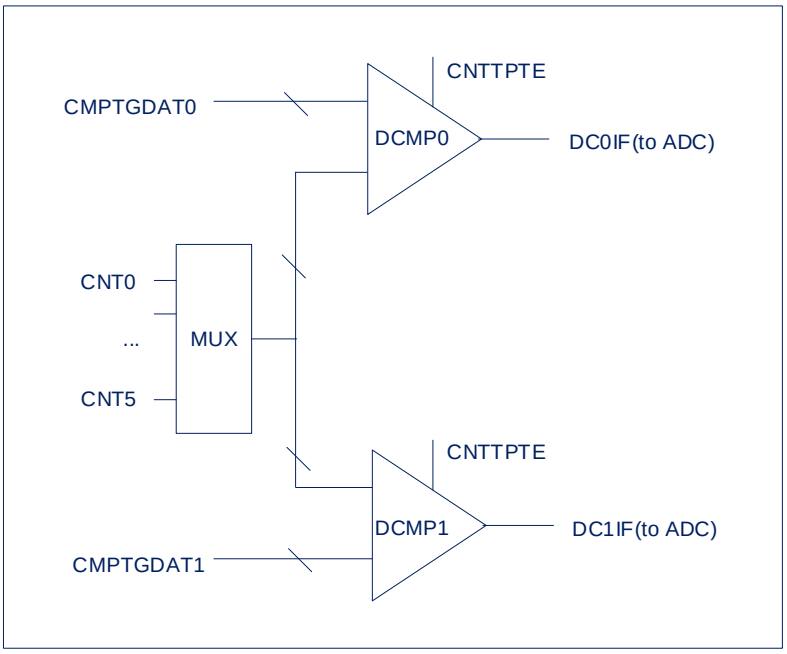


Figure 16-7: Independent counter comparison function

The digital comparator 0 compares the value of the counter CNTn with the value of CMPTGDAT0. If equal, an interrupt flag bit DC0IF is generated, cmPTGD0 [10:8] select one of the PWM0-5 channel counters to compare with CMPTGDAT0.

Digital comparator 1 compares the value of counter CNTn with the value of CMPTGDAT1. If equal, the interrupt flag bit DC1IF is generated CMPTGD1 [10:8] Select one of the PWM0-5 channel counters to compare with CMPTGDAT1

1) Edge alignment mode, how the digital comparator works:

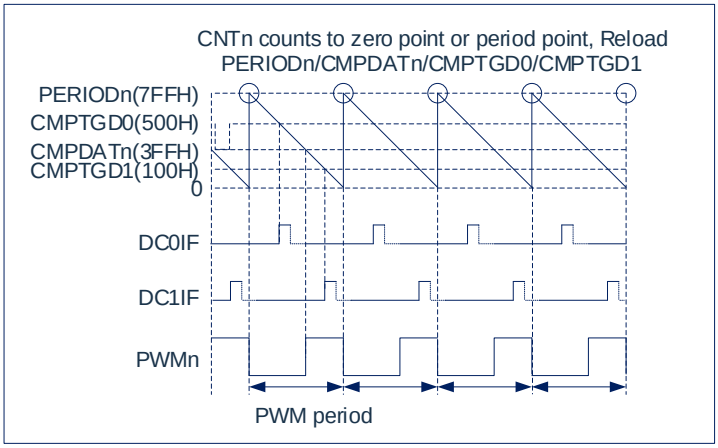


Figure 16-8: Edge alignment mode, how the digital comparator works

In edge counting mode, the digital comparator 0/1 can be set to produce a comparison interrupt at any counting moment.

2) Center alignment mode, how the digital comparator works:

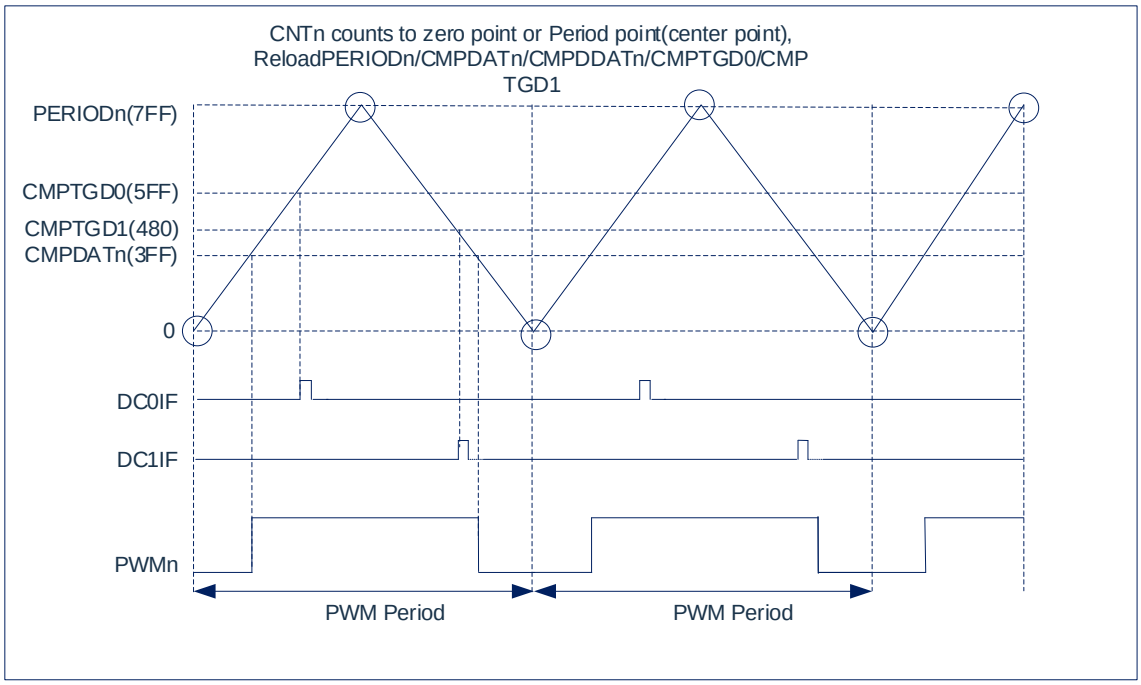


Figure 16-9: Center alignment mode, how the digital comparator works

In center-aligned count mode, the number comparator 0/1 can be set to be triggered by comparison in either up or down count mode. That is, both can be triggered in the first half of the period or the second half of the period, or one can be triggered in the first half of the period and the other in the second half of the period. Determined by CMPTGD0[19] bit CMPTGDSn.

16.3.11 Programmable dead-zone generator

The 6-channel PWM can be set to 3 sets of complementary pairs. In complementary output mode, the period and duty cycles of PWM1, PWM3, and PWM5 are determined by PWM0, PWM2, and PWM4, respectively. The associated register determines, and the dead-zone delay register can also affect the duty cycle of the PWM complementary pair. In addition to the corresponding output enable control bit (PWMnOE), the PWM1/PWM3/PWM5 output waveform is no longer controlled by its own registers.

In complementary mode, each set of complementary PWM pairs supports inserting a dead-zone delay, and the inserted dead-zone time is as follows:

PWM0/1 Dead-zone : (PWM01DT [9:0] +1) *TPWM0

PWM2/3 Dead-zone : (PWM23DT [9:0] +1) * TPWM2

PWM4/5 Dead-zone : (PWM45DT [9:0]+1) *TPWM4

TPWM0/TPWM2/TPWM4 are the clock source periods of PWM0/PWM2/PWM4, respectively.

The dead-zone can be set from 0.021us to 21us (Fpwmn=48MHz).

The output mode does not affect the counter's mode, so both center alignment and edge alignment support complementary output modes.

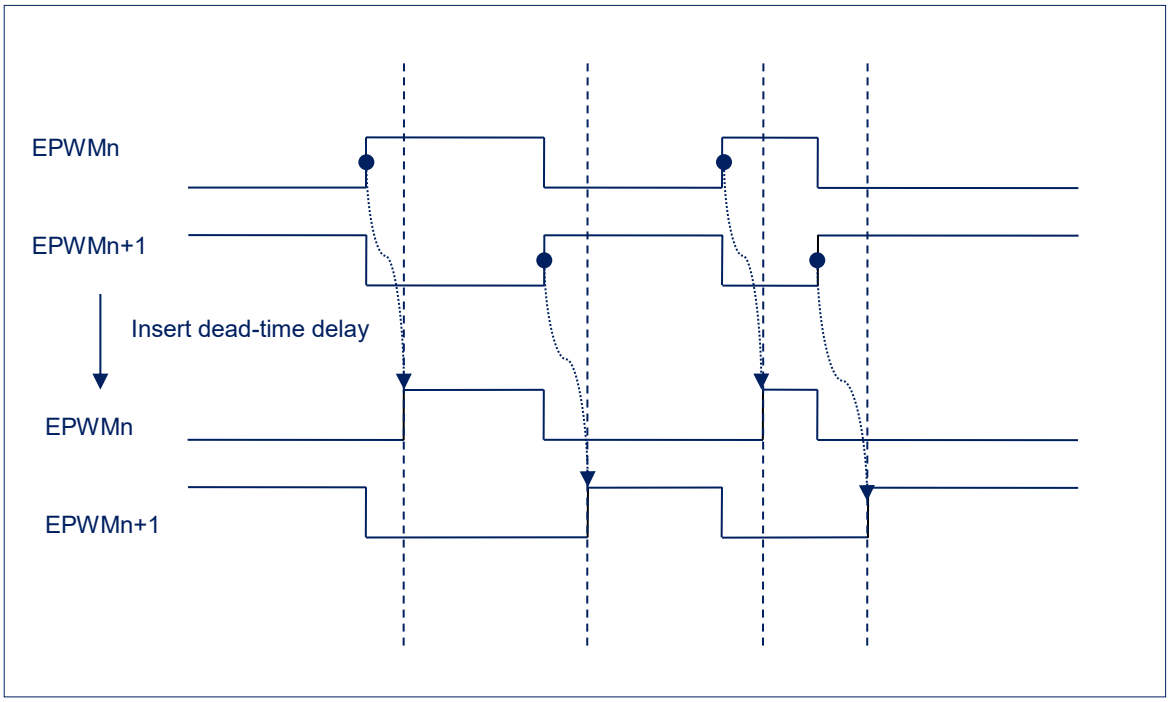


Figure 16-10: Both center alignment and edge alignment support complementary output modes

16.3.12 Mask and mask preset functions

EPWM supports masking functionality. EPWM0-EPWM5 has a separate control for each channel, and the corresponding control bits of EPWMn are MASKENn, MASKDn (in register MASK).

When MASKENn=0, the EPWMn channel outputs a normal PWM waveform;

When MASKENn=1, the EPWMn channel outputs the data of MASKDn;

The mask function's control register, THE MASK, also supports the ability to automatically load preset values. Turning on this function requires the output control register POEN at MASKLE bit set to 1, allowing MASK to automatically load the value of the MASKNXT register while disabling writing to MASK Register.

Load time in POEN MASKLS < 2:0 > setting, with the option to have the same period/duty cycle (load point) as one of epwm0-EPWM5.

16.3.13 Hall sensor interface function

EPWM considers an interface with Hall sensors. An internal HALL position status detection circuit is included that detects the filtered level of the internal capture channels CAP0, CAP1, and CAP2 in the CCP0/1 module.

The presence state after the detection circuit is internally processed is called HALLST:

HALLST has 8 states, which correspond to the HALL position state as follows:

HALLST	The corresponding status
000	Hall detects that the circuit is not started or in its initial state
001	{CAP2-CAP0}=001
010	{CAP2-CAP0}=010
011	{CAP2-CAP0}=011
100	{CAP2-CAP0}=100
101	{CAP2-CAP0}=101
110	{CAP2-CAP0}=110
111	{CAP2-CAP0} The wrong state or sequence of errors during a change

The value of HALLST can be read out from the MASKNXT register, and the HALL position or sequence state can be determined at any time

The HALL status detection sequence supports the following two (the order in which {CAP2, CAP1, CAP0} appears):

- ……-6-2-3-1-5-4-6-……
- ……-6-4-5-1-3-2-6-……

If other sequences are considered to have been errors, HALLST will stop detecting after entering the state of 111. At the same time, the interrupt flag HALLIF will be generated. If you need to restart the HALL detection circuit, you need to write the HALLCLR bit in the MASKNXT register to 1, hallst is from 111 The state enters the initial state of 000 to restart the detection circuit.

Hall detection circuitry provides functionality that can be associated with mask autoloading. This feature does not require software intervention to control the output channel waveform of the EPWM.

HallST corresponds to a mask preset cache for each valid state, for a total of 7 mask preset caches:

HALLST(HALLS=1)	The corresponding mask preset cache
000	Mask preset cache7
001	Mask preset cache 1
010	Mask preset cache 2
011	Mask preset cache 3
100	Mask preset cache 4
101	Mask preset cache 5
110	Mask preset cache 6
111	Mask preset cache7
HALLS=0	Mask preset cache 0

If the mask automatically loads presets is enabled, the data in the corresponding mask preset cache will be loaded into the MASK registers in the corresponding state and at the selected load point. For example:

When the position state in HALLST changes from 000 to 001, the data of the mask preset cache 1 is loaded into the MATRIX register at the first loading point when the 001 state is entered.

After the position state in HALLST changes from 001 to 101, the first load point in the 101 state, the mask preset cache 5 data is loaded into the MASK Registers.

If an incorrect sequence occurs, such as when the CAP2-CAP0 input is changed from 101 to 010, which is not the correct sequence, the position state in HALLST changes from 101 to 111 and set the interrupt flag bit HALLIF to 1. At the first load point of entering the 111 state, the data of the mask preset cache 7 is loaded into the MASK register.

Initially, the data cached by mask preset 7 is loaded into the MASK register at the load point.

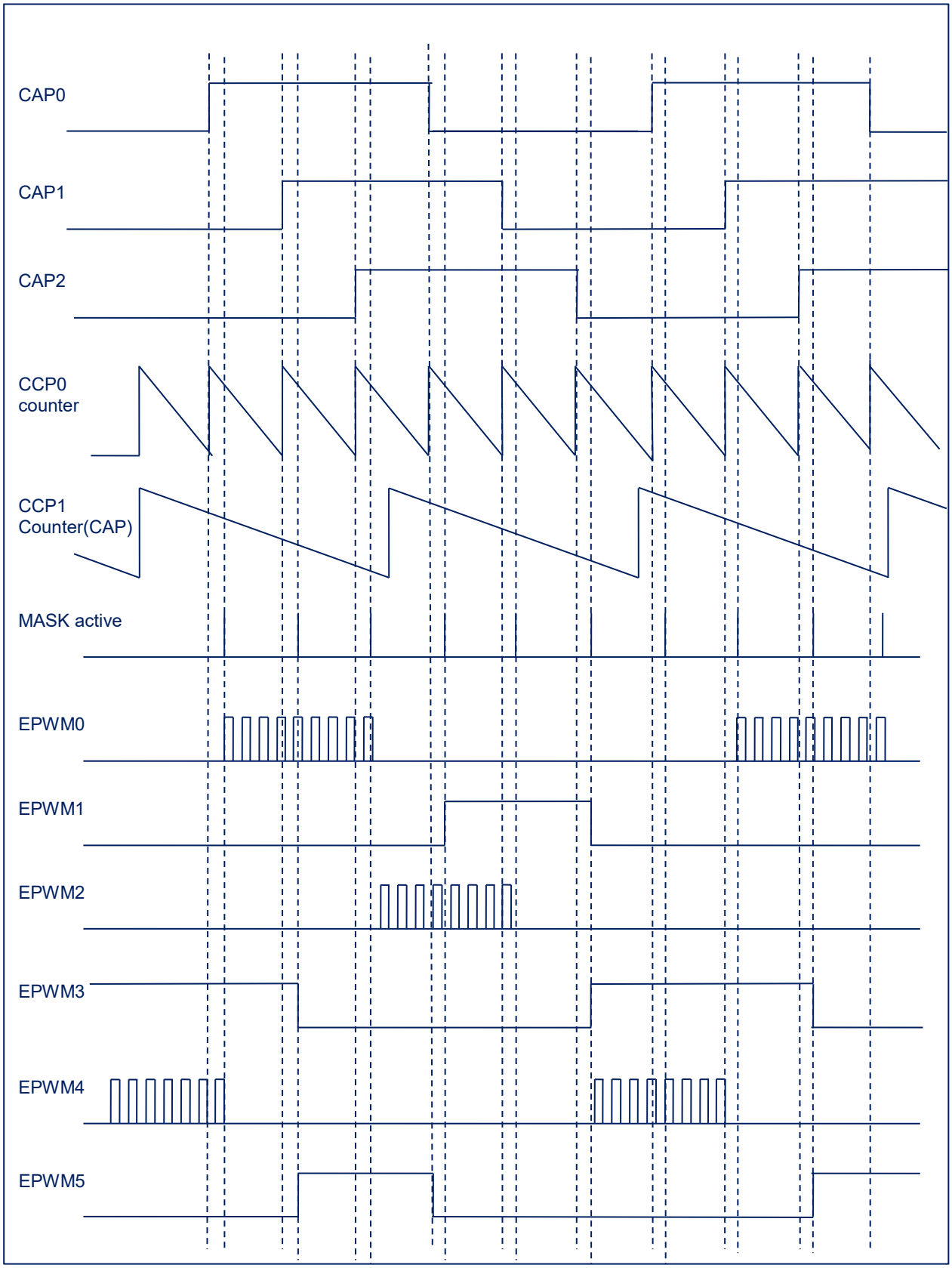


Figure 16-11: Hall detection timing example (not representing the actual running waveform).

16.3.14 Fault protection function (brake and recovery function).

The EPWM supports a fail-safe function, with BKODn controlling the brake thresholds for 6 channels. The fault protection function is controlled by the BRTCTL registers.

EPWM fail-safe trigger sources are:

Level Trigger Source:

1) External BKIN level signal (high or low)
2) Software brake signal (SWBRK bit set to 1)
3) Output of analog comparator 0 (output high or low output)
4) Output of analog comparator 1 (output high or low output)

Pulse trigger source:

1) Edge signal of the external BKIN (rising or falling edge)
2) Analog comparator 0's output event (rising or falling edge or double edge)
3) Analog comparator 1's output event (rising or falling edge or double edge)
4) ADC0 Result Comparator 0 Event (Result Comparison Event)
5) ADCB Result Comparator 0 Event (Result Comparison Event)

Fault interrupt flag bit BRUKIF (software clear 0):

After detecting a valid brake trigger source signal, the fault interrupt flag BRKIF is set to 1 and must be cleared by the software.

Fault signal flag bit BRKAF (read-only):

The fault signal flag is placed at BRKAF at 1, and after the brake signal is revoked, BRKAF automatically clears 0. BRKAF is read-only.

Fault protection output status flag BIT BRKOSF (read-only):

BRKOSF=1, indicating the output BRKODn data status of the EPWMn channel;

BRKOSF=0 indicates that EPWMn is in the normal output state.

Indicates whether the EPWM output is in braking or normal state. When a valid brake signal is detected, the BRKOSF will set 1. In software recovery mode, performing a brake state clear operation (BRKCLR=1) affects the state of this bit.

The fail-safe mode can be divided into 4 types to meet the needs of different fault protection occasions.

BRKMS	Fail-safe mode
00	Stop Mode (Software Recovery)
01	Pause mode (software resume)
10	Recovery Mode (Hardware Recovery)
11	Delayed recovery mode (hardware recovery)

Note: The Fault Interrupt Flag (BRKIF) is independent of the recovery function and only indicates that a brake signal has been generated. Fault interrupt flags also support the accumulation function.

Stop Mode:

Generate fault protection and fault interrupt flags, clear the CNTENn bit, and stop the counter operation. The recovery output requires the brake signal to be revoked, and a fault state clear operation (BRKCLR=1) is performed, and then the CNTENn is reset to 1.

Pause mode:

Fault protection and fault interrupt flags are generated, but the counter continues to operate. Recovery of output requires the brake signal to be revoked, and after performing a fault state clear operation (BRKCLR=1), the output returns to normal at the most recent load update point.

Recovery mode:

Fault protection and fault interrupt flags are generated, but the counter continues to operate. After the brake signal is revoked, the normal output is automatically restored at the last load update point. Failure state cleanup operations are not required.

Attention needs to be paid to distinguishing whether the brake signal is a pulse signal or a level signal: if the brake source is a level signal, you need to wait for the brake to be revoked before you can restore the output; If it is a pulse signal, the EPWM output resumes the output at the last load update point after the start brake, unless the brake pulse signal is generated again during the period.

Delayed recovery mode:

Fault protection and fault interrupt flags are generated, but the counter continues to operate. The brake signal is revoked after a delay for a period of time when the EPWM returns to normal output at the most recent load update point. Failure state cleanup operations are not required.

The delay time can be set freely, and the low 16-bit RDT of the BRKRDT controls the delay time. The delay time is as follows:

$$Tdelay = RDT*T_{APBCLK}$$

Attention needs to be paid to distinguishing whether the brake signal is a pulse signal or a level signal: if the brake source is a level signal, you need to wait for the brake to be revoked before you can restore the output; If it is a pulse signal, the EPWM output waits for the completion delay to resume the output after the last load update point, unless the brake pulse signal is generated again during the period.

After generating brake protection, the EPWMn channel outputs the data in BRKODn, and each channel can set the output high/low level individually.

16.3.15 The output state in debug mode

In debug mode, the state of the CPU has a running state and a paused state. One is the normal operating state; One state is the paused state after executing the TOP command/running to a breakpoint/stepping.

The output state when operating in the pause state EPWM n (POEn=1) can be configured by the HALTMS bit in register CON.

At HALTMS=0, the output state of EPWMn is normal output when paused.

At HALTMS=1, the output state of the EPWMn outputs brake data when paused, but no fault-related flags are generated at this time. The counter for EPWMn will continue to run, and the most recent load update point will resume the EPWMn output after the most recent load update point resumes the run state.

It should be noted that when paused in debug mode, the value of the relevant running data register of EPWMn does not automatically change and remains in its previous state.

16.3.16 Output channel remapping capability

The output channel remapping capability meets the needs of more flexible typography in applications. The pins of EPWM0-EPWM5 in the chip pin distribution chart default to the corresponding PWM channel output. The desired channel can also be reconfigured with the output channel remapping function.

The default internal channels of EPWM0-EPWM5 are IPG0-IPG5, and any channel of IPG0-IPG5 can be redistributed via the EPWM output channel remap register POREMAP EPWMn(n=0-5). The output channel remapping feature only reassigns the port output channels, and its internal controls and interrupts are not remapped.

16.3.17 EPWM configuration process

- Writing 0x55 lock registers enables EPWM register operations
- Configure the EPWM clock divider to set the prescale ratio and independent crossover ratio
- Select Mode, Standalone Mode, or Complementary Mode
- Set the EPWM period and duty cycle
- Sets the EPWM output polarity
- Enables the EPWM counter
- Configure the relevant IO port as the EPWM function port
- Enables the associated EPWM channel output
- Avoid misoperation of the EPWM-related registers 0x00 the LOCK registers are written until the next time the EPWM-related registers need to be operated

16.3.18 interrupt

The EPWM unit has eight interrupt sources:

- ZIFn—Interrupt flag generated when the EPWM counter counts to zero
- UIFn—The EPWM counter counts up to the CMPDATn interrupt flag
- PIFn—The EPWM counter edges align the count interrupt flags and the center aligns the count interrupt flags
- DIFn—The EPWM counter counts down to the CMPDATn/CMPDDATn interrupt flag
- The DC0IF—EPWM counter counts to an interrupt flag equal to CMPTGD0
- The DC1IF—EPWM counter counts to an interrupt flag equal to CMPTGD1
- HALLIF—Hall status error interrupt flag bit
- BRKIF —Fault interrupt flag bit

All interrupt flags are hardware-set and must be cleared by software.

16.4 Register mapping

(EPWM base address = 0x4A80_0000).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
CLKPSC(P1B)	0x000	R/W	EPWM prescaler registers	0x0
CLKDIV(P1B)	0x004	R/W	EPWM clock selection register	0x0
CON(P1B)	0x008	R/W	EPWM control registers	0x0
CON2(P1B)	0x00C	R/W	EPWM control register 2	0x0
CON3(P1B)	0x010	R/W	EPWM control register 3	0x0
PERIOD0(P1A)	0x014	R/W	EPWM period register 0	0x0
PERIOD1(P1A)	0x018	R/W	EPWM period register 1	0x0
PERIOD2(P1A)	0x01C	R/W	EPWM period register 2	0x0
PERIOD3(P1A)	0x020	R/W	EPWM period register 3	0x0
PERIOD4(P1A)	0x024	R/W	EPWM period register 4	0x0
PERIOD5(P1A)	0x028	R/W	EPWM period register 5	0x0
CMPDAT0(P1A)	0x02C	R/W	EPWM comparison register 0	0x0
CMPDAT1(P1A)	0x030	R/W	EPWM comparison register 1	0x0
CMPDAT2(P1A)	0x034	R/W	EPWM comparison register 2	0x0
CMPDAT3(P1A)	0x038	R/W	EPWM comparison register 3	0x0
CMPDAT4(P1A)	0x03C	R/W	EPWM comparison register 4	0x0
CMPDAT5(P1A)	0x040	R/W	EPWM comparison register 5	0x0
POREMAP(P1B)	0x044	R/W	EPWM output channel remap register	0x543210
POEN(P1B)	0x048	R/W	EPWM output control register	0x0
BRKCTL(P1B)	0x04C	R/W	EPWM fail-safe control register	0x0
DTCTL(P1B)	0x050	R/W	EPWM dead-zone length register	0x0
MASK(P1B)	0x054	R/W	EPWM output mask register	0x0
MASKNXT(P1B)	0x058	R/W	EPWM output mask preset register	0x0
CMPTGD0(P1B)	0x05c	R/W	EPWM counter comparison register 0	0x0
CMPTGD1(P1B)	0x060	R/W	EPWM counter comparison register 1	0x0
IMSC(P1B)	0x064	R/W	EPWM interrupt enable register	0x0
RICE	0x068	RO	EPWM interrupt source status register	0x0
PUT	0x06c	RO	EpWM enabled interrupt status register	0x0
ICLR	0x070	WO	EPWM interrupt clear register	0x0
IFA(P1B)	0x074	R/W	EPWM interrupt accumulate control register	0x0
LOCK	0x078	R/W	EPWM write enable control register	0x0
BRKRDT(P1B)	0x07C	R/W	EPWM fault protection recovery delay register	0x0

Note:

1) (P1A/P1B) The registers marked are protected registers.

2) (P1A): When LOCK==55H or AAH, the marked register is allowed to write; = Other values, forbidden to write.

3) (P1B): When LOCK==55H, the labeled register is allowed to write; = Other values, forbidden to write.

16.5 Register description

16.5.1 EPWM Prescale Register (CLKPSC)

bit	symbol	description	Reset value
31:24	-	reserved	-
23:16	CLKPSC45	EPWM counters 4 and 5 clock prescaler CLK_PSC45 = PCLK/(CLKPSC45+1) If the CLKPSC45=0, the prescaler has no clock output, and the CLKDIVn bit does not work if the clock associated with the PSC is selected	0x0
15:8	CLKPSC23	EPWM counters 2 and 3 clock prescaler CLK_PSC23 = PCLK/(CLKPSC23+1) If the CLKPSC23=0 and the prescaler have no clock output, the COUNTER does not work if the CLKDIVn bit selects a clock associated with the PSC	0x0
7:0	CLKPSC01	EPWM counters 0 and 1 clock prescaler CLK_PSC01 = PCLK/(CLKPSC01+1) If the CLKPSC01=0, the prescaler has no clock output, and the CLKDIVn bit does not work if the PSC-related clock is selected	0x0

16.5.2 EPWM Clock Selection Register (CLKDIV)

bit	symbol	description	Reset value
31:23	-	reserved	-
22:20	CLKDIV5	Counter 5 clock divider selection 000: CLK_PSC45/2 001: CLK_PSC45/4 010: CLK_PSC45/8 011: CLK_PSC45/16 100: CLK_PSC45/1 Other values: PCLK	0x0
19	-	reserved	-
18:16	CLKDIV4	Counter 4 clock divider selection 000: CLK_PSC45/2 001: CLK_PSC45/4 010: CLK_PSC45/8 011: CLK_PSC45/16 100: CLK_PSC45/1 Other values: PCLK	0x0
15	-	reserved	-
14:12	CLKDIV3	Counter 3 clock divider selection 000: CLK_PSC23/2 001: CLK_PSC23/4 010: CLK_PSC23/8 011: CLK_PSC23/16 100: CLK_PSC23/1 Other values: PCLK	0x0
11	-	reserved	-
10:8	CLKDIV2	Counter 2 clock divider selection 000: CLK_PSC23/2 001: CLK_PSC23/4 010: CLK_PSC23/8	0x0

		011: CLK_PSC23/16 100: CLK_PSC23/1 Other values: PCLK	
7	-	reserved	-
6:4	CLKDIV1	Counter 1 clock divider selection 000: CLK_PSC01/2 001: CLK_PSC01/4 010: CLK_PSC01/8 011: CLK_PSC01/16 100: CLK_PSC01/1 Other values: PCLK	0x0
3	-	reserved	-
2:0	CLKDIV0	Counter 0 clock divider selection 000: CLK_PSC01/2 001: CLK_PSC01/4 010: CLK_PSC01/8 011: CLK_PSC01/16 100: CLK_PSC01/1 Other values: PCLK	0x0

16.5.3 EPWM Control Register (CON)

bit	symbol	description	Reset value
31:27	-	reserved	-
26	HALTMS	EPWMn channel status control bit when HALT (debug pause). (If POENn=0, the output of EPWMn is high-impedance). 0: Normal output for all channels (POENn=1) 1: Output brake data for all channels (POENn=1) (In the debug state, when running to a breakpoint/step or when paused after operatingthe STOP button, the output of the EPWMn is brake data.) ）	0
25:24	MODE	EPWM operating mode selection 00: Standalone mode 01: Complementary model 10: Synchronous mode 11: reserved	0
23	GROUNPEN	EPWM grouping function enable bit 0: All PWM channels are independent of each other 1: EPWM0 controls EPWM2, EPWM4, EPWM1 controls EPWM3, EPWM5	0
22	ASYMEN	Asymmetric count enablement in EPWM center alignment 1: Symmetry count enables 0: Asymmetric count enablement	0
21	CNTTYPE	EPWM count alignment is selected 0: Edge alignment 1: Center alignment	0
20:19	-	reserved	-
18	EN_DT45	EPWM counters 4 and 5 dead-zone enable bits	0

		0: Disable counters 4 and 5 dead zones 1: Enable counters 4 and 5 dead zones	
17	EN_DT23	EPWM counters 2 and 3 dead-zone enable bits 0: Disable counters 2 and 3 dead zones 1: Enable counters 2 and 3 dead zones	0
16	EN_DT01	EPWM counter 0 and 1 dead-zone enable bits 0: Disable counters 0 and 1 dead zones 1: Enable counters 0 and 1 dead bands	0
15:14	-	reserved	-
13	PINV5	EPWM5 output polarity control bit 0: Normal output 1: Inverting output	0
12	PINV4	EPWM4 output polarity control bits 0: Normal output 1: Inverting output	0
11	PINV3	EPWM3 output polarity control bit 0: Normal output 1: Inverting output	0
10	PINV2	EPWM2 output polarity control bit 0: Normal output 1: Inverting output	0
9	PINV1	EPWM1 output polarity control bit 0: Normal output 1: Inverting output	0
8	PINV0	EPWM0 output polarity control bit 0: Normal output 1: Inverting output	0
7:6	-	reserved	-
5	CNTMODE5	EPWM5 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0
4	CNTMODE4	EPWM4 auto load/single-shot mode 0: Single-shot mode 1: Auto load mode	0
3	CNTMODE3	EPWM3 auto load/single-shot mode 0: Single-shot mode 1: Auto load mode	0
2	CNTMODE2	EPWM2 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0
1	CNTMODE1	EPWM1 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0
0	CNTMODE0	EPWM0 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0

16.5.4 EPWM control register (CON2)

bit	symbol	description	Reset value
31:6	-	reserved	-
5	CNTEN5	EPWM5 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0
4	CNTEN4	EPWM4 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0
3	CNTEN3	EPWM3 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0
2	CNTEN2	EPWM2 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0
1	CNTEN1	EPWM1 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0
0	CNTEN0	EPWM0 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0

16.5.5 EPWM control register (CON3)

bit	symbol	description	Reset value
31	-	reserved	-
30	LETGHALL	The HALL state triggers the LOADENn enable bit 0: Disable 1: Enabling HALL state change triggers LOADENn=1 Note: If the HALL detection state changes, the load enable bit set to 1 for EPWM0-EPWM5 is place 1.	0
29	LETGACMP1	ACMP1 triggers the LOADENn enable bit 0: Disable 1: LOADENn=1 is triggered when ACMP1 is enabled Note: If an ACMP1 event is generated, the LOAD enable bit set to 1 of EPWM0-EPWM5.	0
28	LETGACMP0	ACMP0 triggers the LOADENn enable bit 0: Disable 1: LOADENn=1 is triggered when ACMP0 is enabled	0

		Note: If an ACMP0 event is generated, the EPWM0-EPWM5 load enables bit set to 1.	
27:26	LOADTYP5	EPWM5 load/interrupt mode selection bits 00: Each zero and periodic point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next period point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0
25:24	LOADTYP4	EPWM4 load/interrupt mode select bits 00: Each zero and periodic point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next period point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0
23:22	LOADTYP3	EPWM3 load/interrupt mode selection 00: Each zero and periodic point loads and produces an interrupt flag 01: The first zero point alternates with the next period point to load and produce an interrupt flag 10: Each zero point is loaded with an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0
21:20	LOADTYP2	EPWM2 load/interrupt mode selection 00: Each zero and periodic point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next period point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0
19:18	LOADTYP1	EPWM1 load/interrupt mode selection bits 00: Each zero and periodic point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next period point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0
17:16	LOADTYP0	EPWM0 load/interrupt mode selection 00: Each zero and periodic point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next period point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0
15:14	-	reserved	-
13	LOADEN5	EPWM 5-period/comparator load enable 0: Disable	0

		1: Enable (hardware is automatically clear to zero after loading)	
12	LOADEN4	EPWM4 period/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically clear to zero after loading)	0
11	LOADEN3	EPWM3 period/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically clear to zero after loading)	0
10	LOADEN2	EPWM2 period/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically clear to zero after loading)	0
9	LOADEN1	EPWM1 period/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically clear to zero after loading)	0
8	LOADEN0	EPWM0 period/comparator loading enable bits 0: Disable 1: Enable (hardware is automatically clear to zero after loading)	0
7:6	-	reserved	-
5	CNTCLR5	The EPWM5 counter clears the zero position 0: Disable 1: Enable (hardware auto-zero)	0
4	CNTCLR4	The EPWM4 counter clears the zero position 0: Disable 1: Enable (hardware auto-zero)	0
3	CNTCLR3	The EPWM3 counter is cleared to zero 0: Disable 1: Enable (hardware auto-zero)	0
2	CNTCLR2	The EPWM2 counter clears the zero bit 0: Disable 1: Enable (hardware auto-zero)	0
1	CNTCLR1	The EPWM1 counter clears the zero bit 0: Disable 1: Enable (hardware auto-zero)	0
0	CNTCLR0	The EPWM0 counter clears the zero bit 0: Disable 1: Enable (hardware auto-zero)	0

16.5.6 EPWM period register 0-5 (PERIOD0-5)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:0	PERIODn	EPWMn counter period value	0x0000

16.5.7 EPWM comparision register 0-5 (CMPDAT0-5)

bit	symbol	description	Reset value
31:16	CMPDDATn	The EPWMn counter compares values downwards	0x0000
15:0	CMPDATn	EPWMn counter comparison values	0x0000

16.5.8 EPWM output control register (POEN)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	MASKLE	The EPWM mask control preset data load enable bits 0: Disable 1: Enable (Allows data from the MASKNXT register to be loaded into the MASK register, while writing to the MASK register is prohibited.) In addition, the mask data is not loaded immediately when the bit is 1, and it needs to be loaded at the corresponding loading point)	0
10:8	MASKLS	The EPWM mask control data load moment selection bit 000: Loaded at the load point of EPWM0 001: Loaded at the load point of EPWM1 010: Loaded at the load point of EPWM2 011: Loaded at the load point of EPWM3 100: Loaded at the load point of EPWM4 101: Loaded at the load point of EPWM5 11x: reserved	0
7:6	-	reserved	-
5:0	POENn	EPWMn output enable bit 0: EPWM channel n output is disabled 1: EPWM channel n output enable	0

16.5.9 EPWM Output Channel Remap Register (POREMAP)

bit	symbol	description	Reset value
31:24	PWMRMEN	The EPWM channel remap function enables control AAH: The remap function is enabled EPWMn Which channel output is chosen by PWMnRM Other: The remapping feature is prohibited The EPWMn fixed channel outputs are as follows: EPWM0<- IPG0 EPWM1<- IPG1 EPWM2<- IPG2 EPWM3<- IPG3 EPWM4<- IPG4 EPWM5<- IPG5	0
23	-	reserved	-
22:20	PWM5RM	EPWM channel 5 remap selection bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3	0x5

		100: Map the output of IPG4 101: Map the output of IPG5 11x: reserved	
19	-	reserved	-
18:16	PWM4RM	EPWM channel 4 remap selection bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: reserved	0x4
15	-	reserved	-
14:12	PWM3RM	EPWM channel 3 remap select bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2	0x3
		011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: reserved	
11	-	reserved	-
10:8	PWM2RM	EPWM channel 2 remap select bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: reserved	0x2
7	-	reserved	-
6:4	PWM1RM	EPWM channel 1 remap selects bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: reserved	0x1
3	-	reserved	-
2:0	PWM0RM	EPWM channel 0 remap select bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: reserved	0x0

16.5.10 EPWM Fail-Safe Control Register (BRKCTL)

bit	symbol	description	Reset value
31	BRKEN	EPWM fault protection feature always enables bits 0: Disable (reset fault protection circuit) 1: Enable	0
30	BRKAF	EPWM fault signal flag bit (read-only) 0: No failures were generated 1: Fault signals or brake signals are generated to remain active	0
29:28	BRKMS	EPWM fail-safe mode select bit 00: Stop mode 01: Pause mode 10: Recovery mode 11: Delayed recovery mode Note: When switching fail-safe mode, you must disable the total enable of fail-safe, then switch to the fail-safe mode, and finally turn on the fail-safe total enable bit.	0
27	BRKCLR	EPWM fail-safe clear bit (write only) 0: -- 1: Clear the fail-safe status Note: Only if BRKAF=0 can you write 1, perform a fault cleanup operation, otherwise the operation is invalid.	0
26:24	BRKRCS	EPWM failback load point selection bit 000: Load point recovery for EPWM0 001: Load point recovery for EPWM1 010: Load point recovery for EPWM2 011: Load point recovery for EPWM3 100: Load point recovery for EPWM4 101: Load point recovery for EPWM5 Other: Prohibit selection	0
23	ACMP1BKLE	Analog comparator 1 output level control brake enable bit 0: Disable 1: Enable	0
22	ACMP1BKLS	Analog comparator 1 output level control brake selection 0: Low levels produce brakes 1: High levels produce brakes	0
21	ACMP0BKLE	Analog comparator 0 output level control brake enable bit 0: Disable 1: Enable	0
20	ACMP0BKLS	Analog comparator 0 output level controls brake selection 0: Low levels produce brakes 1: High levels produce brakes	0
19	ACMP1BKEN	Analog comparator 1 output event control brake enable bit 0: Disable 1: Enable (Comparator output event refers to rising/falling/double edge generated, which edge can be selected at ACMP-> CEVCON)	0
18	ACMP0BKEN	Analog comparator 0 output event controls brake enable bits 0: Disable	0

		1: Enable (Comparator output event refers to rising/falling/double edge generated, which edge can be selected at ACMP-> CEVCON)	
17	ADCBMP1BKEN	ADCB comparator 1 outputs brake enable bits 0: Disable 1: Enable	0
16	ADCBMP0BKEN	ADCB comparator 0 output brake enable bit 0: Disable 1: Enable	0
15	--	Must be 0	0
14	ADC0MP0BKEN	ADC0 comparator 0 output brake enable bit 0: Disable 1: Enable	0
13	BRKOSF	EPWM fault protection output status flag bit (read-only) 0: The EPWMn channel is in the normal output state 1: The EPWMn channel is the data state of the output BRKODn	0
12	SWBRK	Software brake enable bit 0: Software brakes are prohibited 1: Immediately generate software brakes	0
11	EXTBRKEE	External hardware brake edges detect enable levels 0: Disable 1: Enable	0
10	EXTBRKES	External hardware brake edges detect selected bits 0: The descending edge triggers the brakes 1: The rising edge triggers the brakes	0
9	EXTBRKLE	External hardware brake level detection enable bit 0: Disable 1: Enable	0
8	EXTBRKLS	External hardware brake level detection select bit 0: Low levels produce brakes 1: High levels produce brakes	0
7:6	-	Must be 0	0
5:0	BRKODn	EPWMn brake output level select bit 0: When the brakes fail, channel n outputs a low level 1: When the brakes fail, channel n outputs high	0

16.5.11 EPWM Dead Zone Length Register (DTCTL)

bit	symbol	description	Reset value
31:30	-	reserved	-
29:20	DTI45	Channel 4 and Channel 5 dead-zone length registers Dead-zone = PWM_CLK45 DTI45×	0x000
19:10	DTI23	Channel 2 and Channel 3 dead-zone length registers Dead-zone = PWM_CLK23 DTI23×	0x000
9:0	DTI01	Channel 0 and channel 1 dead-zone length registers Dead-zone = PWM_CLK01 DTI01×	0x000

16.5.12 EPWM Mask Output Control Register (MASK)

bit	symbol	description	Reset value
31:14	-	reserved	-
13	MASKEN5	EPWM5 mask output enable bits 0: Disable 1: Enable	0
12	MASKEN4	EPWM4 mask output enable bits 0: Disable 1: Enable	0
11	MASKEN3	EPWM3 mask output enable bits 0: Disable 1: Enable	0
10	MASKEN2	EPWM2 mask output enable bits 0: Disable 1: Enable	0
9	MASKEN1	EPWM1 mask output enable bits 0: Disable 1: Enable	0
8	MASKEN0	EPWM0 mask output enable bits 0: Disable 1: Enable	0
7:6	-	reserved	-
5	MASKD5	EPWM5 mask data 0: Output 0 1: Output 1	0
4	MASKD4	EPWM4 mask data 0: Output 0 1: Output 1	0
3	MASKD3	EPWM3 mask data 0: Output 0 1: Output 1	0
2	MASKD2	EPWM2 mask data 0: Output 0 1: Output 1	0
1	MASKD1	EPWM1 mask data 0: Output 0 1: Output 1	0
0	MASKD0	EPWM0 mask data 0: Output 0 1: Output 1	0

16.5.13 EPWM Mask Output Control Preset Register (MASKNXT)

bit	symbol	description	Reset value
31:25	-	reserved	-
24	HALLS	HALL detect mode enable bit 0: Disable 1: Enable	0
23	HALLCLR	HALL error status clear bit 0: Writing 0 is invalid 1: Write 1 to clear the error state of HALLST and return it to the initial state of 000. Read as 0. NOTE 1: If the error status or sequence occurs, HALLST=111, the HALL detection function stops. When the HALL status is enabled again, you need to write 1 to clear the status of 111.	0
22:20	HALLST	Status bits of hall interface (read-only) Detects the status corresponding to {CAP2, CAP1, CAP0} 000: Status is 0 (initial state) 001: The status is 1 010: The status is 2 011: The status is 3 100: The status is 4 101: The status is 5 110: The status is 6 111: Error status Note 1: This state is the status of the HALL interface detected inside the chip, which can be used to determine whether it has entered a valid state, if the status of the three HALL sensors is wrong or the order of the states is wrong, the status bit is 111. Valid Sequence 1: … 6-2-3-1-5-4-6-… Valid Sequence 2: … 6-4-5-1-3-2-6-… Note 2: In a valid status bit, if the mask preset data loading function is enabled, the corresponding mask preset cache data is loaded into the MASK register at the loading point. For example, after hall detection changes to state 3, the first loading point after entering state 3 loads the data of mask preset cache 3 into the MASK register. Note 3: Output data from mask cache 7 in initial state 000 or error state 111.	0
19	-	reserved	-
18:16	PMASKSEL	Mask preset cache selection bits; 000: Select Mask Preset cache 0 001: Select Mask Preset Cache1 010: Select Mask Preset Cache2 011: Select Mask Preset Cache3 100: Select Mask Preset Cache4 101: Select Mask Preset Cache5 110: Select Mask Preset Cache6 111: Select Mask Preset Cache7 Note 1: This selection bit affects the reading and writing of data in the lower 16 bits, and there are 6 mask preset caches inside the EPWM	0

		If 000: Then the register reads and writes data as low as 16 bits for the mask cache 0, If 001: The register reads and writes data as low as 16 bits for the mask cache 1 If 110: The register reads and writes data in cache 6 as low as 16 bits. Note 2: When HALLEN=0, the default loading mask preset cache is 0.	
15:14	-	reserved	-
13	PMASKEN5	The EPWM5 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
12	PMASKEN4	The EPWM4 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
11	PMASKEN3	The EPWM3 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
10	PMASKEN2	The EPWM2 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
9	PMASKEN1	The EPWM1 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
8	PMASKEN0	The EPWM0 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
7:6	-	reserved	-
5	PMASKD5	EPWM5 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
4	PMASKD4	EPWM4 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
3	PMASKD3	EPWM3 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
2	PMASKD2	EPWM2 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
1	PMASKD1	EPWM1 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0
0	PMASKD0	EPWM0 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0

16.5.14 EPWM Trigger Comparison Register (CMPTGD0-1)

bit	symbol	description	Reset value
31:20	-	reserved	-
19	CMPTGDSn	EPWM count comparator n trigger mode (In effect under Center Alignment Count) 0: Triggered when counting down 1: Triggered when counting up	0
18:16	CMPPCHSn	EPWM digital comparator n comparison channel selection 000: Counter of PWM0 001: Counter of PWM1 010: Counter of PWM2 011: Counter of PWM3 100: Counter of PWM4 101: Counter of PWM5 Other values: Counter of PWM0	0
15:0	CMPTGDn	EPWM count comparator n triggers the comparison value	0x0000

16.5.15 EPWM Interrupt Enable Register (IMSC)

bit	symbol	description	Reset value
31	EN_BRKIF	EPWM fault interrupt enable bit 0: Disable 1: Enable	0
30	EN_HALLIF	HALL status Error interrupt enable bit 0: Disable 1: Enable	0
29:24 n=5-0	EN_DIFn	EPWMn down comparision interrupt enable bit 0: Disable 1: Enable	0
23:22	-	reserved	-
21:16 n=5-0	EN_UIFn	EPWMn up comparision interrupt enable bit 0: Disable 1: Enable	0
15	EN_DC1IF	Count comparator 1 interrupt enable bit 0: Disable 1: Enable	0
14	EN_DC0IF	Count comparator 0 interrupt enable bit 0: Disable 1: Enable	0
13:8 n=5-0	EN_PIFn	EPWMn period interrupt enable bit 0: Disable 1: Enable	0
7:6	-	reserved	-
5:0 n=5-0	EN_ZIFn	EPWMn zero-point interrupt enable bit 0: Disable 1: Enable	0

16.5.16 EPWM Interrupt Source Status Register (RIS)

bit	symbol	description	Reset value
31	RIS_BRKIF	EPWM fault interrupt source status bit 0: No interrupt was generated 1: An interrupt has been generated	0
30	RIS_HALLIF	HALL Status Error Interrupt Source Status Bit 0: No interrupt was generated 1: An interrupt has been generated	0
29:24 n=5-0	RIS_DIFn	EPWMn compares the interrupt source status bits downwards 0: No interrupt was generated 1: An interrupt has been generated	0
23:22	-	reserved	-
21:16 n=5-0	RIS_UIFn	EPWMn compares interrupt source status bits upwards 0: No interrupt was generated 1: An interrupt has been generated	0
15	RIS_DC1IF	Count comparer 1 interrupt status bit 0: Disable 1: Enable	0
14	RIS_DC0IF	Count comparer 0 interrupt status bits 0: Disable 1: Enable	0
13:8 n=5-0	RIS_PIFn	EPWMn period interrupt source status bits 0: No interrupt was generated 1: An interrupt has been generated	0
7:6	-	reserved	-
5:0 n=5-0	RIS_ZIFn	EPWMn zero-point interrupt source status bit 0: No interrupt was generated 1: An interrupt has been generated	0

16.5.17 EPWM Enabled Interrupt Status Register (MIS)

bit	symbol	description	Reset value
31	MIS_BRKIF	The EPWM fault enabled interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0
30	MIS_HALLIF	HALL status error enabled interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0
29:24 n=0-5	MIS_DIFn	EPWMn down comparision to the enabled interrupt status bits 0: No interrupt was generated 1: Enabled and produced an interrupt	0
23:22	-	-	-
21:16 n=0-5	MIS_UIFn	EPWMn up comparison has enabled interrupt status bits 0: No interrupt was generated 1: Enabled and produced an interrupt	0
15	RIS_DC1IF	Count Comparer 1 enabled interrupt status bit 0: Disable 1: Enable	0
14	RIS_DC0IF	Count comparator 0 enabled interrupt status bit 0: Disable 1: Enable	0
13:8 n=0-5	MIS_PIFn	The EPWMn period enabled interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0
7:6	-	-	-
5:0 n=0-5	MIS_ZIFn	The EPWMn zero point enabled interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0

16.5.18 EPWM Interrupt Clear Control Register (ICLR)

bit	symbol	description	Reset value
31	ICLR_BRKIF	EPWM fault interrupt clearing control bit Write 0: Does not affect Write 1: Clear the RIS_BRKIF flag bits	0
30	ICLR_HALLIF	HALL status error interrupt clearing control bit Write 0: Does not affect Write 1: Clear the RIS _HALLIF flag bit Note: If HALLST=111, the RIS_HALLIF flag bit cannot be cleared	0
29:24 n=0-5	ICLR_DIFn	EPWMn down comparision the interrupt clear control bit Write 0: Does not affect Write 1: Clear RIS_DIFn flag bits	0
23:22	-	-	-
21:16 n=0-5	ICLR_UIFn	EPWMn up comparision interrupt clearing control bits Write 0: Does not affect Write 1: clear RIS_UIFn flag bits	0
15	ICLR_DC1IF	Count comparator 1 interrupt clearing control bit Write 0: Does not affect	0

		Write 1: Clear RIS_DC1IF flag bits	
14	ICLR_DC0IF	Count comparator 0 interrupt clearing control bit Write 0: Does not affect Write 1: Clear the RIS_DC0IF flag bit	0
13:8 n=0-5	ICLR_PIFn	EpWMn period interrupts the clearning control bit Write 0: Does not affect Write 1: Clear the RIS_PIFn flag bit	0
7:6	-	-	-
5:0 n=0-5	ICLR_ZIFn	EPWMn zero-point interrupt clearing control bit Write 0: Does not affect Write 1: Clear RIS_ZIFn flag bits	0

16.5.19 EPWM Interrupt Accumulation Control Register (IFA)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:12	BRKIFCMP	Fail-safe interrupts accumulate comparison values When fault interrupts accumulate to (BRKIFCMP+1), the BRKIF interrupt flag is at bit set to 1	0x0
11:9	-	reserved	0x0
8	BRKIFAEN	Fail-safe interrupt accumulation enable bits 0: Disable 1: Enable	0x0
7:4	ZIFCMP	Zero-point interrupt accumulates the comparison value When the zero interrupt of the corresponding channel is accumulated to (ZIFCMP+1), the ZIFn interrupt flag bit set to 1 (all channels are the same comparison value)	0x0
3:1	-	reserved	-
0	ZIFAEN	Zero-point interrupt accumulates enable bits 0: Disable 1: Enable	0x0

16.5.20 EPWM Write Enable Control Register (LOCK)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of EPWM other registers; When LOCK=0xaa, only the EPWM period register and the comparison register are enabled; When LOCK=other values, operation of EPWM-related registers is prohibited.	0x0

16.5.21 EPWM Fault Protection Recovery Delay Register (BRKRDT)

bit	symbol	description	Reset value
31:16	-	Must be 0	0x0
15:0	RDT	Fail-safe recovery delay (only delayed recovery mode is valid) Delay time = TRDT $\times_{APBCLK}$	0x0

17. Universal asynchronous transceiver (UART0/1).

17.1 overview

Includes 2 universal asynchronous serial interfaces, supports hardware flow control, software flow control, and supports 16-byte transmit and receive FIFOs.

17.2 characteristic

- Full-duplex, asynchronous communication.
- Independent 16 bytes to send/receive FIFOs.
- Supports hardware automatic flow control (CTS, RTS).
- Support software flow control function (XOFF, XON).
- Optional receive cache trigger level.
- Programmable serial interface features.
  - The data bit length can be set to 5 to 8 bits.
  - The checksums can be set to be parity, no check, or fixed check bits for generation and detection.
  - The stop bit length can be set to 1 bit, 1.5 bits, or 2 bits.

17.3 Feature description

17.3.1 UART function mode

UART is a full-duplex asynchronous communication interface. The UART transceiver each contains a 16-byte FIFO buffer, and the user can set the receive cache trigger level, and can flexibly set the transmit byte length and stop bit length.

Support hardware automatic flow control function (CTS, RTS), and the trigger level of RTS flow control can be set, and the communication parameters of the full-duplex serial interface can be set.

17.3.2 UART interrupts and status

UART supports 7 types of interrupts, including the following:

- Receive interrupts after the threshold level is reached.
- Send a FIFO empty interrupt.
- Line state interrupt (parity error, frame error, interruption interrupt).
- Modem status interrupt.
- Receive buffer timing overflow interrupt.
- Hardware flow interrupt (CTS/RTS).
- Software flow interrupt.

17.4 Register mapping

(UART0 base address = 0x4480_0000; UART1； Base address = 0x4500_0000).

RO: read-only; WO: write only, R/W: read and write;

The x values in the following registers are 0-1.

register	Offset	Read/write	description	Reset value
RBR	0x000	RO	Receive cache registers	-
THR	0x004	WO	Send cache registers	-
DLR	0x008	R/W	Baud rate divider register	0x01
I	0x00c	R/W	Interrupt enable register	0x00
IIR	0x010	RO	Interrupt status register	0x01
FCR	0x014	WO	FIFO control register	0x00
LCR	0x018	R/W	Line control register	0x00
MCR	0x01C	R/W	Modem control register	0x00
LSR	0x020	RO	Line status register	0x60
MSR	0x024	RO	Modem status register	0x00
SCR	0x028	R/W	Cache register	0x00
EFR	0x02C	R/W	Advanced settings register	0x00
XON1	0x030	R/W	XON1 register	0x00
XON2	0x034	R/W	XON2 register	0x00
XOFF1	0x038	R/W	XOFF1 register	0x00
XOFF2	0x03C	R/W	XOFF2 register	0x00

17.5 Register description

17.5.1 Receive Cache Register (RBR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	RBR	A read operation that returns the received data from the FIFO area	-

17.5.2 Send Cache Register (THR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	THR	Writing data to the send buffer, the UART module will send the data at the front end of the FIFO in turn	-

17.5.3 Baud rate divider register (DLR)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:0	DLR	Baud rate = PCLK/16DLR×	0x0001

17.5.4 Interrupt enable register (IER)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	CTSIE	CTS interrupt enable bit (requires AUTOIEN=1 to write). 0: Disable 1: Enable	0
6	RTSIE	RTS interrupt enable bit (requires AUTOIEN=1 to write). 0: Disable 1: Enable	0
5	XOFIE	XOFF interrupt enable bit (requires AUTOIEN=1 to write). 0: Disable 1: Enable	0
4	-	reserved	-
3	MDSIE	Modem status interrupt enable bit 0: Disable 1: Enable	0
2	RLSIE	Receive line status interrupt enable bit 0: Disable 1: Enable	0
1	THREIE	Sends hold register null interrupt enable bits 0: Disable 1: Enable	0
0	RBRIE	Receive data valid interrupt/receive timer overflow interrupt enable bits 0: Disable 1: Enable	0

17.5.5 Interrupt Status Register (IIR)

bit	symbol	description	Reset value
31:6	-	reserved	-
5	INTHFC	Hardware flow control status If the bit is 1, a rising edge is detected at the RTS or CTS pin and can be cleared by reading UARTxIIR	0
4	INTSFC	Software flow control status If the bit is 1, an XOFF character was received. This bit can be cleared by reading the UARTxIIR	0
3:1	INTID	Interrupt status indication 0x0: Modem state changes 0x1: The send hold register is empty 0x2: The received data is valid 0x3: Line status received 0x6: Receive timer overflow	0
0	INT STATUS	Interrupt status 0: At least one interrupt is in the queue 1: There is no interrupt in the queue	1

17.5.6 FIFO Control Register (FCR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:6	RXTL	Receive trigger level, which indicates how many bytes were received before the interrupt was triggered 0x0: Level 0 (1 byte). 0x1: Level 1 (4 bytes). 0x2: Level 2 (8 bytes). 0x3: Level 3 (14 bytes).	0
5:4	TXTL	Send trigger level, which indicates how many bytes were sent to trigger an interrupt (AutoIEN=1 is required to write). 0x0: Level 0 (N-1 bytes, N> = 1 is required, otherwise no interrupt will occur). 0x1: Level 1 (N-4 bytes, N> = 4 is required, otherwise there is no interrupt). 0x2: Level 2 (N-8 bytes, N> = 8 is required, otherwise no interrupt is generated). 0x3: Level 3 (N-14 bytes, N> = 14 is required, otherwise no interrupt is generated). Note: N is the number of bytes written to the FIFO, N< = 17.	0
3	-	reserved	-
2	TXFIFO RST	Send a FIFO reset write 0: Does not affect 1: Clears all data in the sending FIFO and resets the FIFO pointer. The bit clears from zero.	0
1	RXFIFO RST	Receives a FIFO reset write 0: Does not affect 1: Clears all data in the sending FIFO and resets the FIFO pointer. The bit clears from zero.	0
0	FIFOEN	FIFO enable bit 0: FIFO is prohibited 1: Enable FIFO Note: When this bit changes, all data in the sending and receiving FIFOs is automatically cleared	0

17.5.7 Line Control Register (LCR)

bit	symbol	description	Reset value
31:7	-	reserved	-
6	BCON	Break control bit When the bit writes 1 and enables the Break transfer, the TXD port will force the output logic 0	0
5:4	PSEL	Parity bit selection 0x0: Odd checksum, where the odd number of logical 1s is sent and detected in each byte 0x1: For parity, an even number of logical 1s is sent and detected in each byte 0x2: The checksum is forced to 1 0x3: The checksum is forced to be 0	0
3	PEN	The parity enable bit 0: Disables the detection of the generation of checksums 1: Enables the generation and detection of checksums	0
2	SBS	Stop bit selection 0: 1-bit stop bit 1: The stop bit is 1.5 bits when the send word length is 5 bits, and 2 bits when the send word length is other	0
1:0	WLS	The word length selection bit 0x0: 5 digits long 0x1: 6-digit word length 0x2: 7-digit word length 0x3: 8-digit word length	0

17.5.8 Modem Control Register (MCR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	XOFFS	XOFF status bit read only 1: XOFF characters were received 0: XON characters were received	0
6	IRENE	IrDA modem enable bit 0: Disable 1: Enable	0
5	-	reserved	-
4	MLBM	Modem loopback mode 0: Modem loopback mode is disabled 1: Enables Modem loopback mode	0
3:2	-	reserved	-
1	RTS	Modem mode RTS output bits 0: RTS output high 1: RTS output low When modem loopback mode is enabled, the bit is read as 0	0
0	-	reserved	-

17.5.9 Line Status Register (LSR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	RXFE	Receive FIFO error bits (read-only) This bit set to 1 occurs when a receive frame error occurs, a check error, or an interrupting interrupt occurs When there are no errors in the FIFO queue, the bit can be cleared by reading the LSR register	0
6	TEMT	Send cache null flag bit (read-only) 0: The send cache has undelivered data 1: The send cache is empty	1
5	THRE/FIFOE	When FIFOEN=0, it is indicated as a null flag bit (read-only) of the send register 0: The send register has unsent data 1: The send register is empty When FIFOEN=1, it is indicated as sending a FIFO null flag bit (read-only). 0: Sending FIFO has not sent data 1: Send FIFO is empty	1
4	WOULD	Interruption interrupt flag bit (read-only) 0: No interrupt interrupts detected 1: A interrupted interrupt was detected When the UART data input remains low during a transmission (start bit, data, checksum, stop bit), an interrupt interrupt is triggered. The UART remains idle until the data input is high. This bit can be cleared by reading the LSR register	0
3	FE	Frame error flag bit (read-only) 0: No frame errors were detected 1: A frame error was detected This bit can be cleared by reading the LSR register	0
2	ON	Checksum error flag bit (read-only) 0: No checksum errors were detected 1: A checksum error was detected This bit can be cleared by reading the LSR register	0
1	OE	FIFO overflow error flag bit (read-only) 0: No FIFO overflow error detected 1: A FIFO overflow error was detected When the FIFO is full and new data is received, a FIFO overflow error occurs, in which case the data in the FIFO is not overwritten, but the newly received data is lost. This bit can be cleared by reading the LSR register	0
0	RDR	Receive data valid flag bits (read-only) 0: There is no unread data in the receive area 1: There is unread data in the receive area	0

17.5.10 Modem Status Register (MSR)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	CTS	CTS pin status (read-only). 0: The CTS pin input status is low 1: The CTS pin input status is high When moden loopback mode is enabled, the CTS pin status is connected to the MCR[1].	0
3:1	-	reserved	-
0	DCTS	Detects CTS pin level change marker bits (read-only) 0: There is no level change on the CTS input pins 1: The CTS input pins have level variations This bit can be cleared by reading the MSR register	0

17.5.11 Cache register (SCR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	PAD	Read-write 8-bit registers	0x00

17.5.12 Advanced Setup Register (UARTxEFR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	AUTOCTS	Hardware send flow control 0: Disable 1: Enable	0
6	AUTORTS	Hardware receive flow control 0: Disable 1: Enable	0
5	-	reserved	-
4	AUTOIEN	Flow control interrupt enable 0: Disable 1: Enable (Control CTSIE, RTSIE, XOFIE Write Enable)	0
3:2	TXSWFC	Send software flow control bits 0x0: Disable sending software flow control 0x1: Send XON2/XOFF2 as stream control characters 0x2: Send XON1/XOFF1 as stream control characters 0x3: Send XON1 & XON2 and XOFF1 & XOFF2 as stream control characters	0x0
1:0	RXSWFC	Receive software flow control bits 0x0: Disable receiving software flow control 0x1: Receive XON2/XOFF2 as stream control characters 0x2: Receive XON1/XOFF1 as stream control characters 0x3: Receive XON1 & XON2 and XOFF1 & XOFF2 as stream control characters	0x0

17.5.13 XON1, XON2 register (XON1/XON2)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	HXON	XON characters	0x00

17.5.14 XOFF1, XOFF2 register (XOFF1/XOFF2)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	HXOFF	XOFF characters	0x00

18. I2C Serial Interface Controller (I2C)

18.1 overview

I2C is a two-wire bidirectional serial bus that provides a simple and efficient connection for data exchange between devices. I2C is a true multi-master bus that incorporates conflict detection and arbitration mechanisms. Conflict detection and arbitration mechanisms are used to prevent data corruption in cases where two or more hosts are simultaneously trying to control the bus.

18.2 characteristic

- Supports master/slave mode.
- Bidirectional data transfer between master and slave.
- Multi-master bus.
- Simultaneous data arbitration between multiple hosts to avoid serial data corruption on the bus.
- The bus uses a serial synchronous clock that enables different rates between devices.
- Serial synchronous clocks can be used as a handshake mechanism to implement suspend and resume serial transmissions.
- Programmable clocks can be used for a variety of rate controls.
- Supports 7-bit/10-bit slave address modes.
- Supports multi-address recognition (4 groups of slave addresses with mask option).
- Wake-up mode is supported.

18.3 Feature description

18.4 Register mapping

(I2C0 base address = 0x4800_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
CONSET	0x000	R/W	I2C control set register	0x000
CONCLR	0x004	WO	I2C control clear register	0x00
STATE	0x008	RO	I2C status register	0xF8
THAT	0x00C	R/W	I2C data register	0x00
CLK	0x010	R/W	I2C clock control register	0x00
ADR0	0x014	R/W	I2C Slave address register 0	0x00
ADM0	0x018	R/W	I2C Slave address mask register 0	0xFE
XADR0	0x01C	R/W	I2C extend slave address register 0	0x000
XADM0	0x020	R/W	I2C extend slave address mask register 0	0x1FE
RST	0x024	WO	I2C software reset registers	0x00
ADR1	0x028	R/W	I2C Slave Address Register 1	0x00
ADM1	0x02C	R/W	I2C Slave Address Mask Register 1	0xFE
ADR2	0x030	R/W	I2C Slave Address Register 2	0x00
ADM2	0x034	R/W	I2C Slave Address Mask Register 2	0xFE
ADR3	0x038	R/W	I2C Slave Address Register 3	0x00
ADM3	0x03C	R/W	I2C Slave Address Mask Register 3	0xFE

18.5 Register description

18.5.1 I2C Control Set Register (CONSET)

bit	symbol	description	Reset value
31:9	-	reserved	-
8	GCF	I2C broadcasts the call flag bit read only 0: The broadcast call was not received 1: Broadcast call address matching The bit is clear to zero when new data is received or sent	0
7	I2CIE	Interrupt enable bit 0: Disable 1: Enable	0
6	I2CEN	I2C interface enable bit 0: Disable the I2C interface 1: Enables the I2C interface Note: Enables the I2C interface by writing 1 in the I2CEN bit and disables the I2C interface by writing 1 in the I2CENC bit (I2CxCONCLR).	0
5	IS	Startup flag bit Write 1,I2C into host mode and send a start signal; - When I2C is already in host mode, a restart signal is sent. - When I2C is in slave mode, write 1 ends the current transfer and enters master mode while the bus is idle. Write 0 doesn't affect. - When the startup bit or restart bit sending is complete, the bit is automatically zeroed.	0
4	HUNDRED	Stop flag bit When you write 1 in host mode, a stop bit is sent. When writing 1 in slave mode, the I2C module receives a stop bit as if it were received - When the STA and STO are set at the same time, the I2C module sends a stop bit and then a start bit. - When the stop bit sending is complete, the bit is automatically zeroed.	0
3	YES	I2C interrupt flag bit read only When thebus state of I2C changes, this position can be cleared by writing 1 in the SIC bit.	0
2	AA	Reply flag bit 0: No ACK signal was received 1: Reply to the ACK signal in the following cases ● When the slave address matches ● Enables broadcast calls and receives broadcast addresses ● When data is received in master or slave mode, the bit can be zeroed by writing 1 in the AAC bit	0
1	XADRF	I2C slave 10-bit address flag bit read only 0: The I2C address does not match 1: 1^2C 10-bit address matches The bit is clear to zero when new data is sent or received	0
0	ADRF	I2C Slave 7-bit address flag bit, read-only 0: The I2C address does not match 1: 1^2C 7-bit address matches The bit is clear to zero when new data is sent or received	0

18.5.2 I2C Control Clear register (CONCLR)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	I2CIEC	I2C Interrupt disable bit Write 1 clear I2CIE bit Writing 0 does not affect	0
6	I2CENC	The I2C interface disable bit Write 1 clear I2CEN bit Writing 0 does not affect	0
5	STAC	The startup flag clears zero bit Write 1 to zero the STA bit Writing 0 does not affect	0
4	-	reserved	-
3	SIC	The I2C interrupt flag clears zero bit Write 1 clear SI bit Writing 0 does not affect	0
2	AAC	The I2C answer flag clears zero bit Write 1 clear zero AA bit Writing 0 does not affect	0
1:0	-	reserved	-

I2C operations require the appropriate flag bits to be cleared to proceed to the next state.

18.5.3 I2C Status Register (STAT)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	Status	I2C status code 00H: Bus error (valid only in host mode) 08H: Startup bit send complete 10H: Restart bit sending complete 18H: The address + write bit is sent and the ACK is received 20H: Address + write bit sent completed, ACK was not received 28H: In host mode, the data transmission is complete and the ACK is received 30H: The data transmission in host mode is complete and the ACK is not received 38H: Arbitration fails during address or data transfer 40H: Address + read bit sent completed, ACK received 48H: Address + read bit sent completed, ACK was not received 50H: The data is received in host mode and the ACK is replied to 58H: Data is received in host mode and the ACK is not replied to 60H: Receives the address + write bit in the slave mode and replies to the ACK 68H: Host Arbitration fails, slave address + write bit is received, reply ACK 70H: Receive the broadcast call address, reply to the ACK 78H: Host Arbitration fails, receives broadcast call address, reply ACK 80H: After the slave address matches, the data is received and the ACK is replied 88H: After the slave address matches, the data is received and the ACK is not replied 90H: After receiving the broadcast call address from the slave machine, the data is received and the ACK is replied 98H: After receiving the broadcast call address from the slave, the data is received and the ACK is not replied A0H: Receive a stop signal or restart signal in slave mode A8H: Receives the address + read bit in slave mode and replies to the ACK B0H: The host arbitration fails, the slave address + read bit is received, and the ACK is replied B8H: After sending data from machine mode, the ACK is received C0H: After sending data from machine mode, the ACK was not received C8H: After sending the last data in slave mode, the ACK is received D0H: After sending the last data in slave mode, the ACK was not received D8H: Unused E0H: After sending the second address in host mode, the ACK is received E8H: After sending the second address in host mode, the ACK was not received F0H: Unused F8H: Unknown state Other: reserved	0x1F

18.5.4 I2C Data Register (DAT)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	Data	Data received or to be sent	0x00

18.5.5 I2C Clock Control Register (CLK)

bit	symbol	description	Reset value
31:7	-	reserved	-
6:4	M	Sample clock = PCLK/(2^M× (N+1)). SCL clock= PCLK/（2^M×（N+1）×10）	0
3:0	N		0

18.5.6 I2C Slave address register (ADR0/ADR1/ADR2/ADR3)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:1	Address	Slave address	0x00
0	GC	1: Enables broadcast call address recognition 0: Disable broadcast call address recognition	0

18.5.7 I2C Slave address mask register (ADM0/ADM1/ADM2/ADM3)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:1	MASK	Mask bits 0: The bit address is not compared 1: Compare the bit address	0x7F
0	-	reserved	-

18.5.8 I2C Extends the Slave Address Register (XADR0)

bit	symbol	description	Reset value
31:11	-	reserved	-
10:1	Address	10-bit slave address	0x000
0	GC	1: Enables broadcast call address recognition 0: Disable broadcast call address recognition	0

18.5.9 I2C Extended Slave Address Mask Register (XADM0)

bit	symbol	description	Reset value
31:9	-	reserved	-
8:1	MASK	Mask bits 0: The bit address is not compared 1: Compare the bit address	0xFF
0	-	reserved	-

18.5.10 I2C Software Reset Register (RST)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	RST	Writes 0x07, resulting in a software reset	0x00

19. Serial Peripheral Interface Controller (SSP/SPI)

19.1 overview

Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full-duplex mode. The devices can operate in master/slave mode, communicating with each other using a 4-wire bidirectional interface. When receiving data from a peripheral device, SPI performs a serial-to-parallel conversion, and when the data is sent to the peripheral device, it performs a parallel-to-serial conversion. The SPI controller can be configured as either a master or a slave.

19.2 characteristic

- Supports master or slave mode.
- Full duplex.
- The send bit length that can be configured.
- MSB priority send/receive.
- Provides 8 16-bit transmit/receive FIFOs.

19.3 Register mapping

(SSP0 base address = 0x4380_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
WITH	0x000	R/W	SSP control registers	0x000
STATE	0x004	RO	SSP status register	0x03
THAT	0x008	R/W	SSP data registers	0x0000
CLK	0x00C	R/W	SSP clock control registers	0x0000
IMSC	0x010	R/W	SSP interrupt enable register	0x0
RICE	0x014	RO	SSP interrupt source status register	0x8
PUT	0x018	RO	SSP enabled interrupt status register	0x0
ICLR	0x01C	WO	SSP interrupt clear register	0x0
CSCR	0x028	R/W	SSP software chip select signal register	0x00

19.4 Register description

19.4.1 SSP Control Register (CON)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	LBM	Loopback mode enable bit 0: Normal working mode 1: Loopback mode, serial input to serial output	0
10	SSPEN	SSP enable bit 0: Disable 1: Enable	0
9	MS	Master/slave mode select bits 0: Host mode 1: Slave mode	0
8	SOD	The slave output disable bit is valid only in slave mode 0: The SSP can output MISO 1: SSPs cannot output MISOs	0
7	CPH	Clock phase control bit 0: The SSP samples data at the edge of the first clock 1: The SSP samples the data at the second clock edge	0
6	CPO	Clock output polarity select bit 0: SPI_CLK is low when idle 1: SPI_CLK is high when idle	0
5:4	FRF	Frame format 0x0: SPI – Compatible frame format 0x1: TISS – Compatible Frame Format 0x2: Microwire – Compatible frame format 0x3: reserved	0x0
3:0	DSS	Select bits for data transfer length 0x0: reserved 0x1: reserved 0x2: reserved 0x3: 4-digit length 0x4: 5 bits length 0x5: 6 bits length 0x6: 7 bits length 0x7: 8 bits length 0x8: 9 bits length 0x9: 10-bit length 0xA: 11-bit length 0xB: 12-bit length 0xC: 13-bit length 0xD: 14-bit length 0xE: 15-bit length 0xF: 16-bit length	0x0

19.4.2 SSP Status Register (STAT)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	BSY	Busy flag bit, read-only 0: SSP idle 1: The SSP is sending/receiving data or sending FIFO non-null	0
3	RFF	Receives FIFO full flag bits, read-only 0: Receiving FIFO is not full 1: Receiving FIFO is full	0
2	RNE	Receives FIFO non-empty flag bits, read-only 0: The receive FIFO is empty 1: Receive FIFO non-null	0
1	TNF	Sends FIFO non-full flag bits, read-only 0: Send FIFO full 1: Send FIFO not full	1
0	TFE	Sends a FIFO null flag bit, read-only 0: Send FIFO non-empty 1: Send FIFO is empty	1

19.4.3 SSP Data Register (DAT)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:0	DATA	Write data to this register, when there is no data on the bus in the send, the data will be sent out immediately; When there is data on the bus that is being sent, the data is stored in the FIFO and sent sequentially. The minimum interval between send times is 3 SSPCLK clocks. When the data length is less than 16 bits, it needs to be right-aligned. Read this register, read the most recently received data, when the data length is less than 16 bits, need to be right-aligned.	0x0000

19.4.4 SSP Clock Controller (CLK)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:8	M	SSPCLK = PCLK /((M+1)×N) N is an even number of 2-254	0x00
7:0	N		0x00

19.4.5 SSP interrupt enable register (IMSC)

bit	symbol	description	Reset value
31:4	-	reserved	-
3	TXIM	Sends a FIFO interrupt enable bit 0: Disables sending FIFO half-empty interrupts 1: Enables the sending OF FIFO half-empty interrupt	0
2	RXIM	Receives the FIFO interrupt enable bit 0: Disables receiving a HALF-full interrupt from FIFO 1: Enables receive FIFO half-full interrupts	0
1	RTIM	Receives the FIFO timer overflow interrupt enable bit 0: Disables receiving FIFO timer overflow interrupts 1: Enables the receive FIFO timer overflow interrupt (Overflow time: 64×SSPCLK).	0
0	RORIM	Receives the FIFO overflow interrupt enable bit 0: Disables receiving FIFO overflow interrupts 1: Enables receive FIFO overflow interrupts	0

19.4.6 SSP interrupt source status register (RIS)

bit	symbol	description	Reset value
31:4	-	reserved	-
3	TXRIS	This bit is set when sending FIFO is at least half-empty (non-half-empty automatic zeroing)	1
2	RXRIS	This bit is set when the receive FIFO is at least half full (non-half full auto clear)	0
1	RTRIS	This bit is set when the receive FIFO is not empty and not read till timeout	0
0	RORRIS	When the receive FIFO is full and another frame of data is received, the old data is lost	0

19.4.7 SSP enabled interrupt status register (MIS)

bit	symbol	description	Reset value
31:4	-	reserved	-
3	TXMIS	This bit is set when the enables the transmit FIFO in half-empty, and the transmit FIFO is at least half-empty	0
2	RXMIS	This bit is set when the receive FIFO is half full interrupt and the receive FIFO is at least half full	0
1	RTMIS	When the enable receive FIFO timer overflow interrupts and the receive FIFO is not empty, the timeout is not read when the bit is not read	0
0	RORMIS	This bit is set when the receive FIFO overflow interrupt is enabled, and the receive FIFO is full, and a frame of data is received,	0

19.4.8 SSP Interrupt Clear register (ICLR)

bit	symbol	description	Reset value
31:2	-	reserved	-
1	RTIC	Write 1 to clear the RTRIS flag bit	0
0	RORIC	Write 1 to zero the RORRIS flag bit	0

19.4.9 SSP Software Chip Select Signal Register (CSCR)

bit	symbol	description	Reset value
31:5	-	reserved	-
4	SPH	Select the signal from the machine chip 0: After each frame of data transmission is completed, the chip selection signal cannot be pulled high 1: After each frame of data transmission is completed, the chip selection signal must be pulled high	0
3	SWCS	Software chip select signal control bit in host mode 0: Output low 1: Output high	0
2	SWSEL	Select signal selection in host mode 0: The chip selection signal is automatically controlled by the SPI module 1: The chip selection signal is controlled by the SWCS bit	0
1:0	-	reserved	-

20. Low Speed Analog-to-Digital Conversion (ADC0)

20.1 overview

The chip contains a 12-bit, 20 channel successive approximation analog-to-digital converter (ADC).

20.2 characteristic

- Analog input voltage range: AVSS(VSS) ~ AVDD(VDD).
- Maximum sampling rate: 100Ksps.
- Up to 20 single-ended analog input channels.
- Single conversion time: 18.5*T_{ADCK}.
- Single-shot mode: Performs an A/D conversion on the specified channel.
- Continuous mode: A/D conversion is performed on all selected channels.
- Supports an external input signal to trigger an ADC conversion.
- Supports interrupt after conversion is complete.
- Built-in AD conversion result comparator.
- The conversion results for each channel are stored in the corresponding data registers.
- Channels 12-20 test dedicated analog voltage signals (op0/1 output port, PGA0/1 output port, temperature sensor, internal reference, ADC reference positive). /negative end, etc.).

20.3 Feature description

20.3.1 ADC channel description

ADC channel number	ADC channel	Priority	Description
0	AN0_0	highest	ADC channel 0
1	AN0_1		ADC channel 1
2	AN0_2		ADC channel 2
…	…		-
n	AN0_n		ADC channel n
…	…		-
11	AN0_11		ADC channel 11
12	ThePO_O		The output of OP0 (port input to ADC).
13	TheP1_O		The output of OP1 (port input to ADC).
14	PGA0_O		The output of PGA0 (port input to ADC).
15	PGA1_O		The output of PGA1 (port input to ADC).
16	Bandgap(1.2V)		-
17	TS		The output of the temperature sensor
18	AVDD(VDD)		Positive reference voltage
19	AVSS(VSS)	minimum	Negative reference voltage

Note: AN0_0-AN19 any combination of channels supports continuous mode conversion

20.4 Register mapping

(ADC base address = 0x4300_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
ADCCON(P1B)	0x000	R/W	ADC control register	0x0
ADCCON2(P1B)	0x004	R/W	ADC control register 2	0x0
ADCHWTG(P1B)	0x008	R/W	ADC hardware trigger control registers	0x0
--	0x00C	--	--	0x0
ADCSCAN(P1B)	0x010	R/W	ADC scan register	0x0
ADCCMP0(P1B)	0x014	R/W	ADC comparator 0 control register	0x0
--	0x018	R/W	--	0x0
ADCIMSC(P1B)	0x01C	R/W	ADC interrupt enable register	0x0
ADCRIS	0x020	RO	ADC interrupt source status register	0x0
ADCMIS	0x024	RO	The ADC enabled interrupt status register	0x0
ADCICLR	0x028	WO	ADC interrupt clear register	0x0
ADCLOCK	0x02C	R/W	The ADC write enable control register	0x0
--	--	--	--	--
ADCDATA0	0x080	RO	ADC channel 0 conversion result register	0x0
ADCDATA1	0x084	RO	ADC channel 1 conversion result register	0x0
ADCDATA2	0x088	RO	ADC channel 2 conversion result register	0x0
ADCDATA3	0x08C	RO	ADC channel 3 conversion result register	0x0
ADCDATA4	0x090	RO	ADC channel 4 conversion result register	0x0
ADCDATA5	0x094	RO	ADC channel 5 conversion result register	0x0
ADCDATA6	0x098	RO	ADC channel 6 conversion result register	0x0
ADCDATA7	0x09C	RO	ADC channel 7 conversion result register	0x0
ADCDATA8	0x0A0	RO	ADC channel 8 conversion result register	0x0
ADCDATA9	0x0A4	RO	ADC channel 9 conversion result register	0x0
ADCDATA10	0x0A8	RO	ADC channel 10 conversion result register	0x0
ADCDATA11	0x0AC	RO	ADC channel 11 conversion result register	0x0
ADCDATA12	0x0B0	RO	ADC channel 12 conversion result register	0x0
ADCDATA13	0x0B4	RO	ADC channel 13 conversion result register	0x0
ADCDATA14	0x0B8	RO	ADC channel 14 conversion result register	0x0
ADCDATA15	0x0BC	RO	ADC channel 15 conversion result register	0x0
ADCDATA16	0x0C0	RO	ADC channel 16 conversion result register	0x0
ADCDATA17	0x0C4	RO	ADC channel 17 conversion result register	0x0
ADCDATA18	0x0C8	RO	ADC channel 18 conversion result register	0x0
ADCDATA19	0x0CC	RO	ADC channel 19 conversion result register	0x0

Note:

1. The registers marked (P1B) are protected registers.
2. (P1B): When LOCK==55H, the labeled register is allowed to write; = Other values, forbidden to write.

20.5 Register description

20.5.1 ADC Control Register (ADCCON)

bit	symbol	description	Reset value
31:14	-	reserved	-
13	ADCSWCHE	The ADC channel software enable bit 0: Automatically turned on by hardware 1: The open channel is determined by ADCSWCHS	0
12:5	-	reserved	0
4	ADCEN	The ADC enable control bit 0: Disable 1: Enable	0
3	ADCMS	ADC mode select bit 0: Single conversion 1: Continuous conversion	0
2:0	ADCDIV	ADC clock prescaler selection bit F_{ADC} = PCLK/2^{ADCDIV}	0

20.5.2 ADC Control Register 2 (ADCCON2)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	ADCST	ADC conversion begins (the hardware is automatically clear to zero after the conversion ends). 0: The conversion is over or the ADC is in idle mode (Writing 0 is invalid). 1: Start the conversion (ADCEN must be 1).	0
6:5	-	reserved	-
4:0	ADCSWCHS	ADC channel software select bit (requires ADCSWCHE=1 to take effect). 00000 Select Channel 0 00001 Select Channel 1 …… …… 10011 Select Channel 19 other reserved	0

20.5.3 ADC Scan Register (ADCSCAN)

bit	symbol	description	Reset value
31:20	-	reserved	0
19:0	ADCEn	ADC channel n enable bit (n=19-0). 0: Disable 1: Enable	0

20.5.4 ADC Hardware Trigger Control Register (ADCHWTG)

bit	symbol	description	Reset value
31:18	-	reserved	-
17	ADCEXTAT	ADC external trigger enable bit 0: Disable 1: Enable	0
16	ADCEXTES	ADC external trigger edge selection bit 0: Falling edge 1: Rising edge	0
15	ADCINTTGEN	The ADC internal function trigger enable bit 0: Disable 1: Enable	0
14:12	ADCINTTGSS	The internal function of the ADC trigger source channel selection bit 000: ADC0 converts the end signal 001: ADCB converts the end signal 010: ACMP0 event 011: ACMP1 event 100: Timer0 Interrupt Signal 101: Timer1 Interrupt Signal 110: Timer2 Interrupt Signal 111: Timer3 Interrupt Signal	0
11:0	-	reserved	-

20.5.5 ADC conversion result register (ADCDATAx) (x=0~19).

bit	symbol	description	Reset value
31:12	-	reserved	-
11:0	RSLT	ADC conversion result	0x0

20.5.6 ADC compares control register 0 (ADCCMPx) (x=0).

bit	symbol	description	Reset value
31	ADCCMPxEN	ADC comparator x enable bit 0: - 1: Enable	0
30	ADCCMPxO	ADC comparator x result bits (read-only) (The selected channel is automatically updated after conversion is completed). 0: The conditions for comparison are not met 1: The comparison criteria are met	0
29:	-	reserved	-
28	ADCCMPxCOND	ADC comparator x compares conditional selection bits 0: ADC results < presets 1: ADC result > = preset	0
27:24	ADCCMPxMCNT	ADC comparator x number of matches preset When the analog-to-digital conversion result of the specified channel matches the comparison condition, the internal counter is incremented by 1, and when the internal counter is equal to the value of ADCCMPxMCNT+1, the internal counter value is automatically cleared. If the match condition is not met during the accumulation process, the value of the internal	0

		counter is also automatically cleared to zero, that is, the accumulation process has a filtering function. An ADC comparison event is generated at the same time as the match. Note: - ADC Comparator 0 Compare Event will place the interrupt flag ADCCMP0IF as 1;	
23:21	-	reserved	0
20:16	ADCCMPxCHS	ADC comparator x compares channel selection bits 00000- Channel 0 …… …… 10011- Channel 19 Other- reserved	0
15:12	-	reserved	-
11:0	ADCCMPxDATA	ADC comparator x data preset (12 bits).	0

20.5.7 ADC Interrupt Enable Register (ADCIMSC)

bit	symbol	description	Reset value
31	ADCIMSC31	ADC comparator 0 interrupt enable bit 0: Disable 1: Enable	0
30:20	-	reserved	0
19:0	ADCIMSCn	ADC channel n interrupt enable bit (n=19-0). 0: Disable 1: Enable	0

20.5.8 ADC Interrupt Source Status Register (ADCRIS)

bit	symbol	description	Reset value
31	ADCRIS31	ADC comparator 0 interrupt source state 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0
30:20	-	reserved	0
19:0	ADCRISn	ADC channel n interrupt source state (n=19-0). 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0

20.5.9 ADC Enabled Interrupt Status Register (ADCMIS)

bit	symbol	description	Reset value
31	ADCMIS31	ADC comparator 0 interrupt state 0: No interrupt was generated 1: Enables and produces an interrupt	0
30:20	-	reserved	0
19:0	ADCMISn	ADC channel n interrupt state (n=19-0). 0: No interrupt was generated 1: Enables and produces an interrupt	0

20.5.10 ADC Interrupt Clear register (ADCICLR)

bit	symbol	description	Reset value
31	ADCICLR31	Write 1 clear ADC comparator 0 interrupt state Writing 0 does not affect	0
30:20	-	reserved	0
19:0	ADCICLRn	Write 1 to clear the ADC channel n interrupt status Writing 0 does not affect (n=19-0).	0

20.5.11 ADC Write Enable Control Register (LOCK)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of the ADC-related registers (See ADC Register Mapping For details). When LOCK=other values, operation of ADC-related registers is prohibited	0

21. Fast analog-to-digital conversion (ADCB)

21.1 overview

The chip contains a 12-bit, 20-channel fast successive approximation analog-to-digital converter (ADCB).

21.2 characteristic

- Analog input voltage range: AVSS(VSS/AVREFN) ~ AVDD (VDD/AVREFP).
- Maximum sampling rate: 1.2Msps.
- Up to 20 single-ended analog input channels.
- Two power modes are supported: high-speed mode and low-current mode.
- Single sampling and conversion time in high-speed mode: 52*T_{ADCK} (sampling time set to 1 3.5*T_{ADCK}).
- Single-shot mode: Performs an A/D conversion on the specified channel.
- Continuous mode: A/D conversion is performed on all selected channels.
- Supports an external input signal to trigger an ADC conversion.
- Supports interrupt after conversion is complete.
- Built-in AD conversion result comparator.
- The conversion results for each channel are stored in the corresponding data registers.
- Channels 12-20 test dedicated analog voltage signals (op0/1 output port, PGA0/1 output port, temperature sensor, internal reference, ADC reference positive/negative terminal, etc.).

21.3 Feature description

21.3.1 Channel of the ADC

ADC channel number	ADC channel	ADC channel priority	Description
0	AN1_0	highest	External channel 0
1	AN1_1		External channel 1
2	AN1_2		External channel 2
…	…		-
n	AN1_n		External channel n
…	…		-
11	AN1_11		External channel 11
12	OP0_O (port signal).		The output of OP0
13	OP1_O (port signal).		The output of OP1
14	PGA0_O (port signal).		The output of PGA0
15	PGA1_O (port signal).		The output of PGA1
16	Bandgap(1.2V)		Internal reference output
17	TS		The output of the temperature sensor
18	VDD/AVREFP		Positive reference voltage
19	VSS/AVREFN	minimum	Negative reference voltage

Note: The AN0-AN19 any combination of channels supports continuous mode conversion.

21.3.2 Power mode of the ADC

There are two types of ADC operating modes: high-speed mode and low-current mode.

High-speed mode: This mode converts faster.

Low Current Mode: This mode transitions slightly slower and the operating current of the ADC decreases significantly. For applications with low slew rate requirements, this mode can be used to reduce the power consumption of the ADC. The successive comparison time in this mode is 10 cycles T_{ADCK} more than in high-speed mode.

21.3.3 The conversion mode of the ADC

There are two types of ADC conversion modes: single-shot conversion mode and continuous conversion mode.

Single-shot conversion mode:

The operation ends after a conversion of the channel with the highest enabled priority and produces an interrupt flag.

Continuous conversion mode:

The operation ends after all enabled channels are converted and an interrupt flag is generated, and the disabled channels are ignored and skipped.

When ADCSWCHE=0, software channel opening is disabled, and the selection and opening of ADC channels is automatically controlled by hardware.

When ADCSWCHE = 1, the software channel is enabled, the selection and opening of the ADC channel is controlled by ADCSWCHS, and after ADCSWCHS selects a channel, the channel is automatically opened (ADCEN must be 1). Single-shot mode and continuous mode actually convert the channel selected by ADCSWCHS under this condition.

21.3.4 The clock of the ADC

The clock of the ADC is derived from the APB clock, which can be configured with a choice of 8 dividers 1/2/4/8/16/32/64/128 via ADCDIV.

Time of AD conversion of single-shot mode in high-speed mode (T_{ADC}):

$2*T_{ADCK}$ (default switching settling time) $+13.5*T_{ADCK}$ (default sampling time) $+31.5*T_{ADCK}$ (successive comparison time) $+5*T_{ADCK}$

The time at which a single AD conversion (TDC) is completed in continuous conversion mode in high-speed mode mode:

$2*T_{ADCK}$ (default switching settling time)$+13.5*T_{ADCK}$ (default sampling time)$+31.5*T_{ADCK}$ (successive comparison time) $+3*T_{ADCK}$

At ADCSWCHE=1, the actual switching settling time is selected to a certain channel and the time from the start of the conversion.

21.3.5 ADC software start

Writing 1 in register ADCCON2.ADCST bit initiates the ADC conversion. After the conversion is complete, the bit hardware is automatically cleared to zero.

During an ADC conversion, any software and hardware triggering start signals are ignored.

21.3.6 The ADC hardware trigger start

Trigger Source:

In addition to software-initiated conversion, ADCs can also trigger ADC conversions through hardware. The types of hardware trigger sources are:

1) External triggering
2) Internal triggering
3) EpWM output channel triggering
4) EPWM count comparator 0 triggered
5) EPWM Count Comparator 1 triggered

Different types of trigger sources can be valid at the same time, the same kind of trigger sources may contain different trigger signals, such as EPWM output channel trigger, you can choose one of the EPWM0-EPWM5 trigger signal.

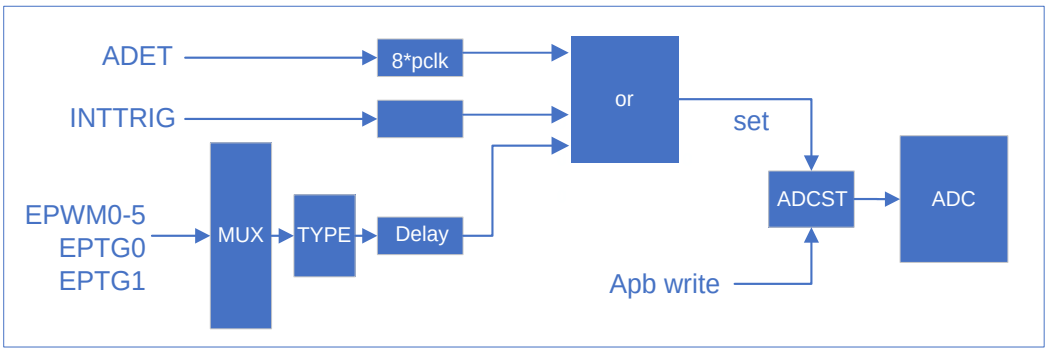


Figure21-1: ADC hardware triggers boot

External trigger:

External trigger can choose to start the ADC on the rising or falling edge, after detecting the external trigger signal, after filtering by 2 PCLK clocks, the ADCST will be set to 1 to start the ADC conversion.

Internal trigger:

Internal triggers include: ADC0, ADCB, ACMP0, ACMP1, TIMER0/1/2/3 triggers.

ADC0: The conversion of ADC0 ends

ADCB: The conversion of ADCB ends

ACMP0: The event output of ACMP0

ACMP1: The event output of ACMP1

Timer0: Enabled Interrupt for Timer0 (TMR0MIS)

Timer1: Enabled Interrupt for Timer1 (TMR1MIS)

Timer2: Enabled interrupt for Timer2 (TMR2MIS)

Timer3: Enabled Interrupt for Timer3 (TMR3MIS)

EPWM output channel triggering:

EPWM output channel trigger can select the rising edge, falling edge, zero, period point to start the ADC, if the EPWM trigger signal is detected, you can choose to start the ADC conversion after a certain delay. If the output channel of EPWM is remapped, the EPWM trigger signal is the signal before remapping, ipGn signal.

EPWM output channel triggering allows individual ADC conversion channels to be set. That is, after the EPWM output channel trigger signal is generated, it will be converted according to the unique configured channel. The conversion channel

of the EPWM output channel that triggers the ADC is set in the ADCCHEPWM register. After the conversion is complete, it will revert to the channel settings in ADCSCAN.

EPWM counter comparator trigger:

The EPWM count comparator 0/1 trigger can be set to trigger the start-up ADC at any time during the EPWMn period in the same way as the EPWM channel trigger, or it can choose to start the ADC conversion after a certain delay.

The EPWM count comparator 0/1 trigger allows individual ADC conversion channels to be set. That is, after the trigger signal is generated, it will be converted according to the individual setting channel. The EPWM count comparator 0 triggers the conversion channel of the ADC set in the ADCCHEPTG0 register. The conversion channel of the EPWM count comparator 1 triggering the ADC is set in the ADCCHEPTG1 register.

After the conversion is complete, it will revert to the channel settings in ADCSCAN.

EPWM trigger delay:

The ADCEPWMTGDLY register determines when EPWM triggers the start ADC delay:

(ADCEPWMTGDLY[9:0]+2)*PCLK (Zero/EPWM Comparator 0/EPWM Comparator 1)

(ADCEPWMTGDLY [9:0]+3)*PCLK (rising/falling edge/period point)

The range of EPWM trigger delay is as follows:

PCLK	48MHz	64MHz
Delay	0.02us~21.4us	0.02us~16us

If ADCPWMTGDLY=0, the ADC conversion is initiated by delaying one PCLK clock.

21.3.7 EPWM triggers the initiation of the ADC configuration

EPWM-triggered ADC conversion has special time requirements in some applications. For this requirement, the ADC supports different EPWM trigger conditions within the ADC to set up independent conversion channels. For example:

EPWM output channel triggering selects AN0, AN1, AND2 channel conversion.

EPWM comparator 0 triggers selectable AN18 channel conversion.

EPWM comparator 1 triggers selectable AN19 channel conversion.

The channels for software startup or other trigger start selection are AN5, AN6, AN7, AN8.

When there is no EPWM trigger condition, the default conversion channel is AN5-AN8.

If the OUTPUT channel of EPWM is triggered, only 3 channels of AN0-AN2 will be selected for AD conversion, and the CONVERSION will be automatically switched to AN5-AN8 channel enable.

If the EPWM's comparison 0 is triggered, only the AN18 channel is selected for AD conversion, and after the conversion is completed, it is automatically switched to AN5-AN8 channel enable.

If the COMPARISON 1 of epgwm is triggered, only the AN19 channel is selected for AD conversion, and after the conversion is completed, it is automatically switched to AN5-AN8 channel enable.

It is important to note that any other trigger signals will be ignored during the period when the AD conversion is not finished.

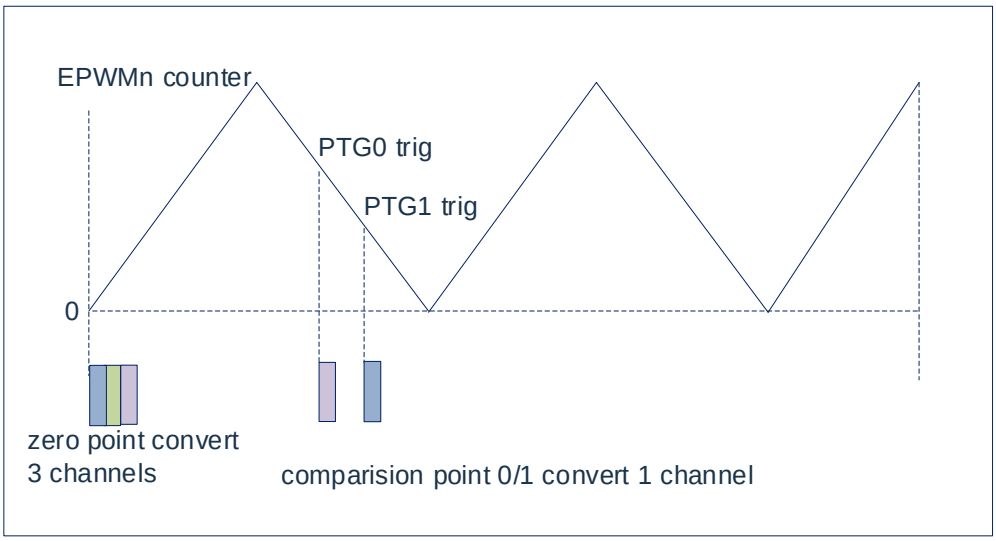


Figure 21-2: EPWM triggers to start the ADC setup

Note:

- The channel that triggers the ADC enable conversion at zero is determined by ADCCHPEM;
- The conversion channel at point 0 that triggers the ADC enable is determined by ADCCHPTG0;
- The conversion channel that triggers the ADC enable at point 1 is determined by ADCCHPTG1;
- The conversion channel that initiates the ADC enable in other ways is determined by ADCCAN.

21.4 Register mapping

(ADCB base address = 0x4D80_0000) RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
CON(P1B)	0x000	R/W	ADC control register	0x000D000
CON2(P1B)	0x004	R/W	ADC control register 2	0x0
HWTG(P1B)	0x008	R/W	ADC hardware trigger control register	0x0
PWMTGDLY(P1B)	0x00C	R/W	ADC EPWM trigger delay data register	0x0
SCAN(P1B)	0x010	R/W	ADC scan register	0x0
CMP0(P1B)	0x014	R/W	ADC comparator 0 control register	0x0
CMP1(P1B)	0x018	R/W	ADC comparator 1 control register	0x0
IMSC(P1B)	0x01C	R/W	ADC interrupt enable register	0x0
RICE	0x020	RO	ADC interrupt source status register	0x0
PUT	0x024	RO	ADC enabled interrupt status register	0x0
ICLR	0x028	WO	ADC interrupt clear register	0x0
LOCK	0x02C	R/W	ADC write enable control register	0x0
CHEPWM(P1B)	0x030	R/W	ADC EPWM output trigger conversion channel register	0x0
CHPTG0(P1B)	0x034	R/W	ADC EPWM comparator 0 trigger conversion channel register	0x0
CHPTG1(P1B)	0x038	R/W	ADC EPWM comparator 1 trigger conversion channel registe	0x0
--	--	--	--	--
TEST(P1B)	0x048	R/W	ADC test register	0x0
--	--	--	--	--
DATA0	0x080	RO	ADC channel 0 conversion result register	0x0
DATA1	0x084	RO	ADC channel 1 conversion result register	0x0
DATA2	0x088	RO	ADC channel 2 conversion result register	0x0
DATA3	0x08C	RO	ADC channel 3 conversion result register	0x0
DATA4	0x090	RO	ADC channel 4 conversion result register	0x0
DATA5	0x094	RO	ADC channel 5 conversion result register	0x0
DATA6	0x098	RO	ADC channel 6 conversion result register	0x0
DATA7	0x09C	RO	ADC channel 7 conversion result register	0x0
DATA8	0x0A0	RO	ADC channel 8 conversion result register	0x0
DATA9	0x0A4	RO	ADC channel 9 conversion result register	0x0
DATA10	0x0A8	RO	ADC channel 10 conversion result register	0x0
DATA11	0x0AC	RO	ADC channel 11 conversion result register	0x0
DATA12	0x0B0	RO	ADC channel 12 conversion result register	0x0
DATA13	0x0B4	RO	ADC channel 13 conversion result register	0x0
DATA14	0x0B8	RO	ADC channel 14 conversion result register	0x0
DATA15	0x0BC	RO	ADC channel 15 conversion result register	0x0
DATA16	0x0C0	RO	ADC channel 16 conversion result register	0x0
DATA17	0x0C4	RO	ADC channel 17 conversion result register	0x0
DATA18	0x0C8	RO	ADC channel 18 conversion result register	0x0
DATA19	0x0CC	RO	ADC channel 19 conversion result register	0x0

Note:

1) The registers marked (P1B) are protected registers.

2) (P1B): When LOCK==55H, the labeled register is allowed to write; = Other values, forbidden to write.

21.5 Register description

21.5.1 ADC Control Register (CON)

bit	symbol	description	Reset value
31	ADCRST	The ADC module reset control bits 0: --- 1: ADC module reset	0
30:26	-	Reserved, must be 0	0
25:24	ADMODE10	ADC power mode select bit 00: High-speed mode 01: Reserved, prohibits selection 10: Reserved, prohibits selection 11: Low current mode	0
23:16	ADCNSMP	ADC internal sampling time selection bit 00000000: reach 00000100: Prohibit selection 00000101: 5.5 ADC clock cycles 00000110: 6.5 ADC clock cycles 00000111: 7.5 ADC clock cycles 00001000: 8.5 ADC clock cycles 00001001: 9.5 ADC clock cycles 00001010: 10.5 ADC clock cycles 00001011: 11.5 ADC clock cycles 00001100: 12.5 ADC clock cycles 00001101: 13.5 ADC clock cycles 00001000: … 111111110: 254.5 ADC clock cycles 111111111: 255.5 ADC clock cycles	0x0D
15:14	-	Must be 0	0
13	ADCSWCHE	The ADC channel software enable bit 0: Automatically turned on by hardware 1: Channel opening is determined by ADCSWCHS	0
12	ADCNDISEN	ADC charge-discharge function selection bit 0: discharge 1: charge	0
11:8	ADCNDISTS	ADC charge-discharge time selection bit 0000: No charging or discharging 0001: Prohibit selection 0010: 2 ADC clock cycles 0011: 3 ADC clock cycles … 1111: 15 ADC clock cycles	0
7:6	ADCVS	The ADC positive reference selection bit 00: Select VDD 01: Select AVREFP 10: Choose BG(1.2V) 11: Prohibit selection	0
5	ADCGS	ADC negative-end reference select bit	0

		0: Select VSS 1: Select AVREFN	
4	ADCEN	The ADC enable control bit 0: Disable 1: Enable	0
3	ADCMS	ADC conversion mode selection bit 0: Single conversion 1: Continuous conversion (After converting all enabled ADC channels at once, the order is channels 0 to 19, and the hardware of the channel without enable is automatically ignored, and no conversion operation is generated)	0
2:0	ADCDIV	ADC clock prescaler selection bit F_{ADC} = PCLK/2^{ADCDIV}	0

21.5.2 ADC Control Register 2 (CON2)

bit	symbol	description	Reset value
31:12	-	reserved	-
11	ADCSF4	ADC Transition Status Flag Bit 4 (Read Only) 0: - 1: A single conversion is complete	0
11	ADCSF3	ADC Transition Status Flag Bit 3 (Read Only) 0: - 1: The conversion is complete before the ADC clock cycles	0
10	ADCSF2	ADC Transition Status Flag Bit 2 (Read Only) 0: - 1: The conversion is complete with the first two ADC clock cycles	0
9	ADCSF1	ADC Transition Status Flag Bit 1 (Read Only) 0: - 1: During conversion	0
8	ADCSF0	ADC Transition Status Flag Bit 1 (Read Only) 0: - 1: During sampling	0
7	ADCST	ADC conversion starts (hardware is automatically clear to zero after conversion) 0: The conversion is over or the ADC is in idle mode (Invalid to write 0) 1: Start the conversion (ADCEN must be 1)	0
6	ADCSMPWAIT	ADC sampling time extends the control bit 0: - 1: Force the sampling state to be maintained during sampling	0
5	-	Reserved, must be 0	-
4:0	ADCSWCHS	The ADC channel software selects the select bit (ADCSWCHE=1 is required to take effect) 00000: Select Channel 0 00001: Select Channel 1 … 10011: Select Channel 19 other reserved	0

21.5.3 ADC Hardware Trigger Control Register (HWTG)

bit	symbol	description	Reset value
31:18	-	reserved	-
17	ADCEXTEN	ADC external trigger enable bit 0: Disable 1: Enable	0
16	ADCEXTES	ADC external trigger edge selection bit 0: Falling edge 1: Rising edge	0
15	ADCINTTGEN	The ADC internal function triggers the enable bit 0: Disable 1: Enable	0
14:12	ADCINTTGSS	The internal function of the ADC triggers the source channel selection bit 000: ADC0 converts the end signal 001: ADCB conversion end signal 010: ACMP0 event 011: ACMP1 event 100: Timer0 Interrupt Signal 101: Timer1 Interrupt Signal 110: Timer2 Interrupt Signal 111: Timer3 Interrupt Signal	0
11:10	-	reserved	-
9	ADCPTG1EN	ADC EPWM Count Comparator 1 triggers the enable bit 0: Disable 1: Enable	0
8	ADCPTG0EN	ADC EPWM count comparator 0 trigger enable bit 0: Disable 1: Enable	0
7	ADCEPWMTEN	ADC EPWM output trigger enable bit 0: Disable 1: Enable	0
6:4	ADCEPWMTSS	The ADC EPWM output trigger source channel selection bit 000: The trigger source is EPWM0 001: The trigger source is EPWM1 010: The trigger source is EPWM2 011: The trigger source is EPWM3 100: The trigger source is EPWM4 101: The trigger source is EPWM5 11x: reserved	0
3:2	-	reserved	-
1:0	ADCPEWMTPS	ADC EPWMn trigger mode select bit (n=0-5) 00: The rising edge of the EPWMn waveform 01: EPWMn Periodic Point (IPGn) 10: The falling edge of the EPWMn waveform 11: Zero point of EPWMn (IPGn)	0

21.5.4 ADC EPWM Trigger Delay Register (EPWMTGDLY)

bit	symbol	description	Reset value
31:10	-	reserved	-
9:0	ADCEPWMTGDLY	ADC EPWM triggers delay data EPWM trigger delay (including output channel triggering with EPWM comparator 0/1) (ADCPWMTGDLY+2) *PCLK After initiating the ADC conversion (set the ADCST to 1) (ADCEPWMTGDLY=0, delay is 1*PCLK)	0

21.5.5 ADC Scan Register (SCAN)

bit	symbol	description	Reset value
31:20	-	reserved	-
19:0	ADCEn	ADC channel n enable bit (n=19-0) 0: Disable 1: Enable	0

21.5.6 ADC EPWM Output Trigger Conversion Channel Enable Register (CHEPWM)

bit	symbol	description	Reset value
31:20	-	reserved	-
19:0	ADCCHEPWMn	ADC EPWM output trigger conversion channel enable bit (n=19-0) 0: Disable 1: Enable	0

21.5.7 ADC EPWM Comparator 0 Trigger Conversion Channel Enable Register (CHPTG0)

bit	symbol	description	Reset value
31:20	-	reserved	-
19:0	ADCCHPTG0n	ADC EPWM comparator 0 trigger conversion channel enable bit (n=19-0) 0: Disable 1: Enable	0

21.5.8 ADC EPWM Comparator 1 Trigger Conversion Channel Enable Register (CHPTG1)

bit	symbol	description	Reset value
31:20	-	reserved	-
19:0	ADCCHPTG1n	ADC EPWM Comparator 1 Trigger Conversion Channel Enable Bit (n=19-0) 0: Disable 1: Enable	0

21.5.9 ADC Test Register (TEST)

bit	symbol	description	Reset value
31:24	ADCSWT	ADC analog switch toggle delay time: (i.e. from the time the analog switch is turned on to the start of sampling) （ADCSWT+2）ADC clock cycles Note: It is recommended to extend this time when performing ADC conversion of weak signals	0
23:0	-	Reserved, must be 0	-

21.5.10 ADC conversion result register (DATAx) x=0~19

bit	symbol	description	Reset value
31:12	-	reserved	-
11:0	RSLT	ADC conversion result	0x0

21.5.11 ADC comparision control register 0 (CMPx) x=0 to 1

bit	symbol	description	Reset value
31	ADCCMPxEN	ADC comparator x enable bit 0: - 1: Enable	0
30	ADCCMPxO	ADC comparator x result bits (read-only) (The selected channel is automatically updated after the conversion is complete) 0: The conditions for comparison are not met 1: The comparison criteria are met	0
29	-	reserved	-
28	ADCCMPxCOND	ADC comparator x compares conditional selection bits 0: ADC results < presets 1: ADC result > = preset	0
27:24	ADCCMPxMCNT	ADC comparator x number of matches preset When the analog-to-digital conversion result of the specified channel matches the comparison condition, the internal counter is incremented by 1, and when the internal counter is equal to the value of ADCCMPxMCNT+1, the internal counter value is automatically cleared. If the match condition is not met during the accumulation process, the internal counter value is automatically cleared to zero, that is, the function has a filtering function. Matching generates an ADC comparison event that can be used as a signal to trigger the brake action of the EPWM. Note: - The ADC Comparator 0 comparison event will place the interrupt flag - ADCCMP0IF is 1;	0
23:21	-	reserved	-
20:16	ADCCMPxCHS	ADC comparator x compares channel selection bits 00000: Channel 0 …… …… 10011: Channel 19 Other: reserved	0
15:12	-	reserved	-
11:0	ADCCMPxDATA	ADC Comparator x Data Presets (12 bits)	0

21.5.12 ADC Interrupt Enable Register (IMSC)

bit	symbol	description	Reset value
31	ADCIMSC31	ADC comparator 0 interrupt enable bit 0: Disable 1: Enable	0
30:20	-	reserved	0
19:0	ADCIMSCn	ADC channel n interrupt enable bit (n=19-0) 0: Disable 1: Enable	0

21.5.13 ADC Interrupt Source Status Register (RIS)

bit	symbol	description	Reset value
31	ADCRIS31	ADC comparator 0 interrupt source state 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0
30:20	-	reserved	0
19:0	ADCRISn	ADC channel n interrupt source state (n=19-0) 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0

21.5.14 ADC Enabled Interrupt Status Register (MIS)

bit	symbol	description	Reset value
31	ADCMIS31	ADC comparator 0 interrupt state 0: No interrupt was generated 1: Enables and produces an interrupt	0
30:20	-	reserved	-
19:0	ADCMISn	ADC channel n interrupt state (n=19-0) 0: No interrupt was generated 1: Enables and produces an interrupt	0

21.5.15 ADC Interrupt Clear register (ICLR)

bit	symbol	description	Reset value
31	ADCICLR31	Write 1 clear ADC comparator 0 interrupt state Writing 0 does not affect	0
30:20	-	reserved	-
19:0	ADCICLRn	Write 1 clear ADC channel n interrupt status (n=19-0) Writing 0 does not affect	0

21.5.16 ADC Write Enable Control Register (LOCK)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of the ADC-related registers (See Registered ADC Memory Mapping For details). When LOCK=other values, operation of ADC-related registers is prohibited	0

22. Operational amplifier (OP0/1, PGA0/1)

22.1 overview

The chip contains two basic op amp blocks and two programmable gain amplifiers. A small number of peripheral components can be used to achieve basic signal amplification and signal calculation functions.

22.2 characteristic

OP (Operational Amplifier)

- Each op amp is multiplexed on all three ends with the GPIO port.
- The positive side selects the BandGap (1.2V) input.
- Configurable to comparator mode.
- The OP0/1 output ports have dedicated ADC channels AN0_ 12/13 and AN1_12/13 connected to ADC0 and ADCB, respectively.

PGA (Programmable Gain Amplifier)

- Adjustable gain: 4X/8X/10X/12X/14X/16X/32X.
- Two inputs on the positive end.
- Pseudo-differential architecture is supported, and feedback can be selected from an external port.
- The PGA0/1 output port has dedicated ADC channels AN0_14/15 and AN1_14/15 to ADC0 and ADCB, respectively.

22.3 Function description

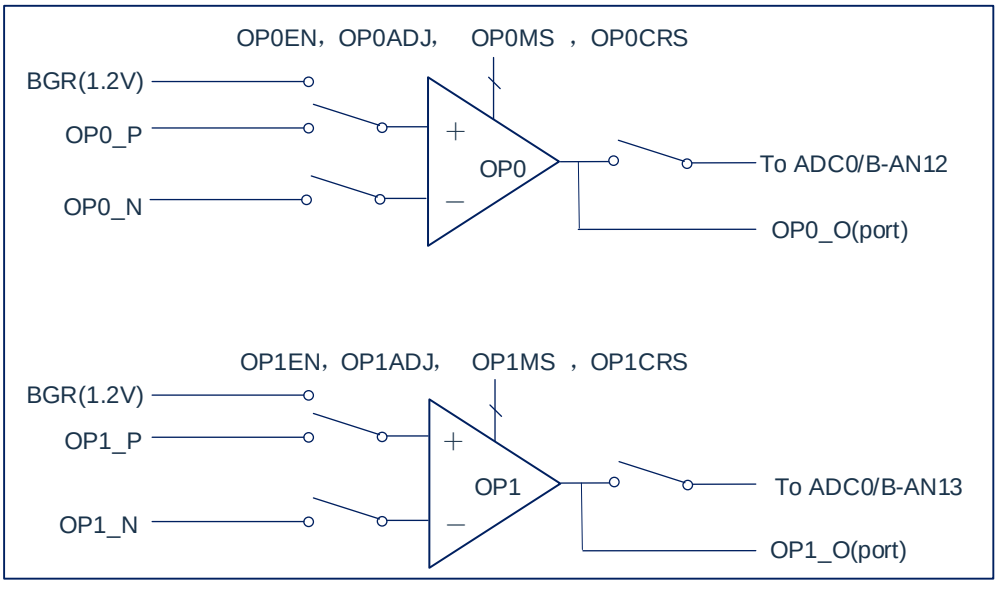


Figure 22-1: Op Amp vs. PGA Structure Diagram (1).

OPnEN=1, the OPn_O port output function takes effect automatically, so the relevant port must be configured as an analog port before configuring op amp enable.

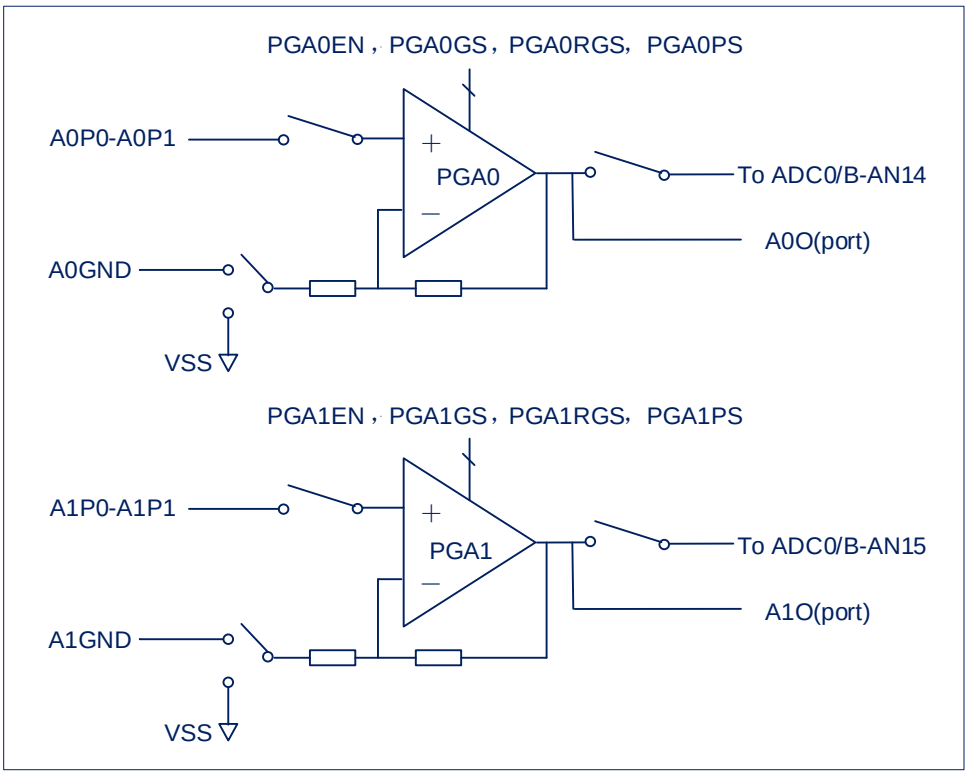


Figure 22-2: Op Amp and PGA Structure Diagram (2).

At PGAnEN=1, the AnO port output function takes effect automatically, so the relevant port must be configured as an analog port before configuring PGA enable.

22.4 Register mapping

(OP0 base address = 0x4C80_0000; OP1 base address = 0x4C80_000C).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
WITH0	0x000	R/W	OP control register 0	0x0
CON1	0x004	R/W	OP control register 1	0x10

(PGA0 base address = 0x4C80_0018; PGA1 base address = 0x4C80_0024).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
WITH	0x000	R/W	PGA control registers	0x0

22.5 Register description

22.5.1 Op amp n control register 0 (CON0) (n=0-1)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	OPnEN	Op amp n enable bit 0: Disable 1: Enable	0
6:5	OPnMS	Op amp n operating mode selection 00: Op Amp mode 01: Compare mode 10: Adjustment mode 0, positive and negative shorts and internal ground 11: Mode 1, shorted positive and negative terminals, can input common-mode levels from the port OPnCRS=0 select input from the negative side OPnCRS=1 selected from the positive input	0
4	-	Must be 0	0
3:2	OPnNS	Op amp n negative channel selection bit 00: OPn_N Other: forbidden	0
1:0	OPnPS	Op amp n positive channel selection bit 00: OPn_P 01: 1.2V(Bandgap) Other: forbidden	0

22.5.2 Op amp n control register 1 (CON1) (n=0-1)

bit	symbol	description	Reset value
31:8	-	reserved	-
7	OPnOUT	Op amp n adjusts the resulting bit/comparator mode output (read-only)	0
6	OPnCRS	Op amp n mode input select bit 0: Negative-side input 1: Positive input	0
5:0	-	reserved	-

22.5.3 PGAn control register 0 (CON) (n=0-1)

bit	symbol	description	Reset value
31:16	-	reserved	-
15	PGAnEN	PGAn enable bit 0: Disable 1: Enable	0
14:12	PGAnGS	PGAn gain select bit 000: 4x 001: 8x 010: 10x 011: 12x 100: 14x 101: 16x 11x: 32x	0
11	PGAnRGS	PGAn feedback resistor ground selection 0: connected to internal ground 1: Connect to the AnGND port	0
10:6	-	Reserved, must be 0	0
5:4	PGAnPS	PGAn positive channel selection bit 00: AnP0 01: AnP1 1x: Reserved, prohibits selection	0
3:0	-	reserved	-

23. Analog comparator (ACMP0/1)

23.1 overview

Inside the chip are two analog comparators. The comparator can be configured for different applications. When the positive voltage is greater than the negative voltage, the comparator outputs logic 1 and vice versa output 0, which can also be changed by the output polarity select bit. When the comparator output value changes, each comparator can be configured to generate an interrupt.

23.2 characteristic

- Analog input voltage range: 0 ~ (VDD-1.5V).
- Supports unilateral/bilateral hysteresis.
- Hysteresis voltage selection (10mV/20mV/60mV-typ) is supported.
- Each comparator positive terminal can select 4 port inputs with OP0/1, PGA0/1 output ports.
- Each comparator negative terminal can select the port input and internal reference voltage.
- The internal reference voltage VREF selects the divider output of the internal Bandgap (1.2V) and VDD.
- Internal reference voltage divider range: (2/20)*VREF~(17/20)*VREF has a total of 16 gears to choose from.
- Output filterable time can be selected: 0 ~ 512 * Tsys.
- The comparator event output can be used as a brake trigger signal for the enhanced PWM.
- Output changes can produce interrupts.

23.3 Function description

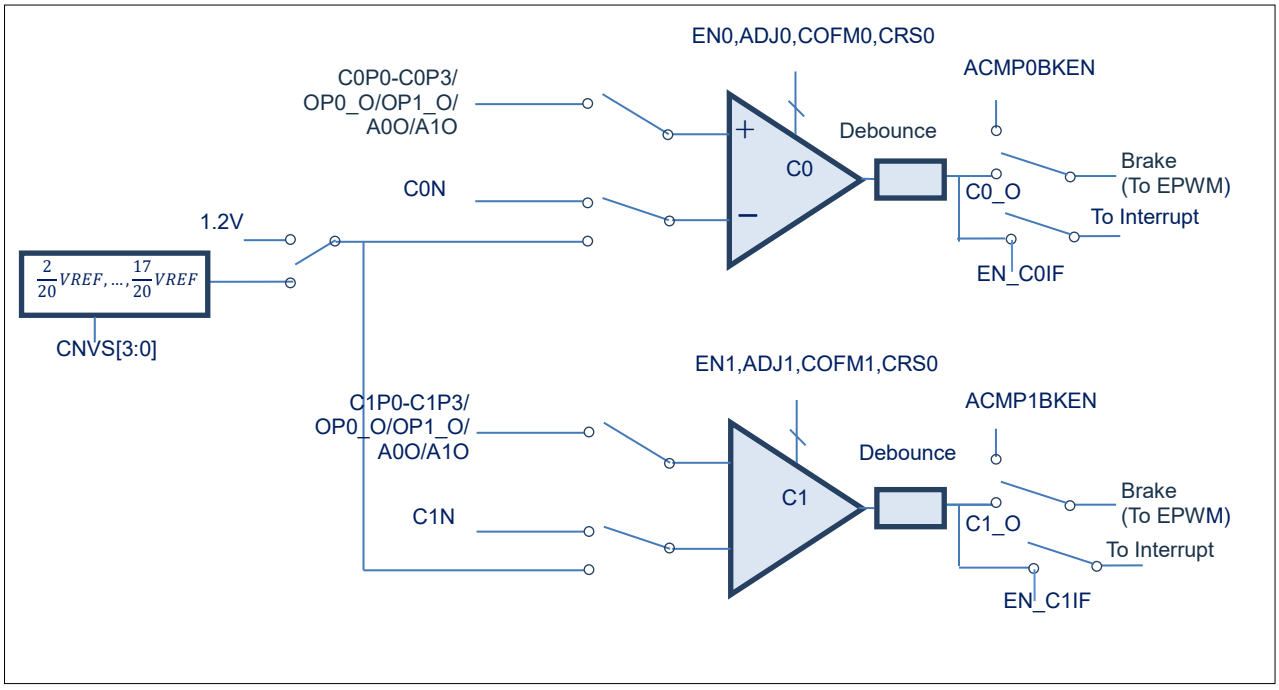


Figure 23-1: Comparator Block Diagram

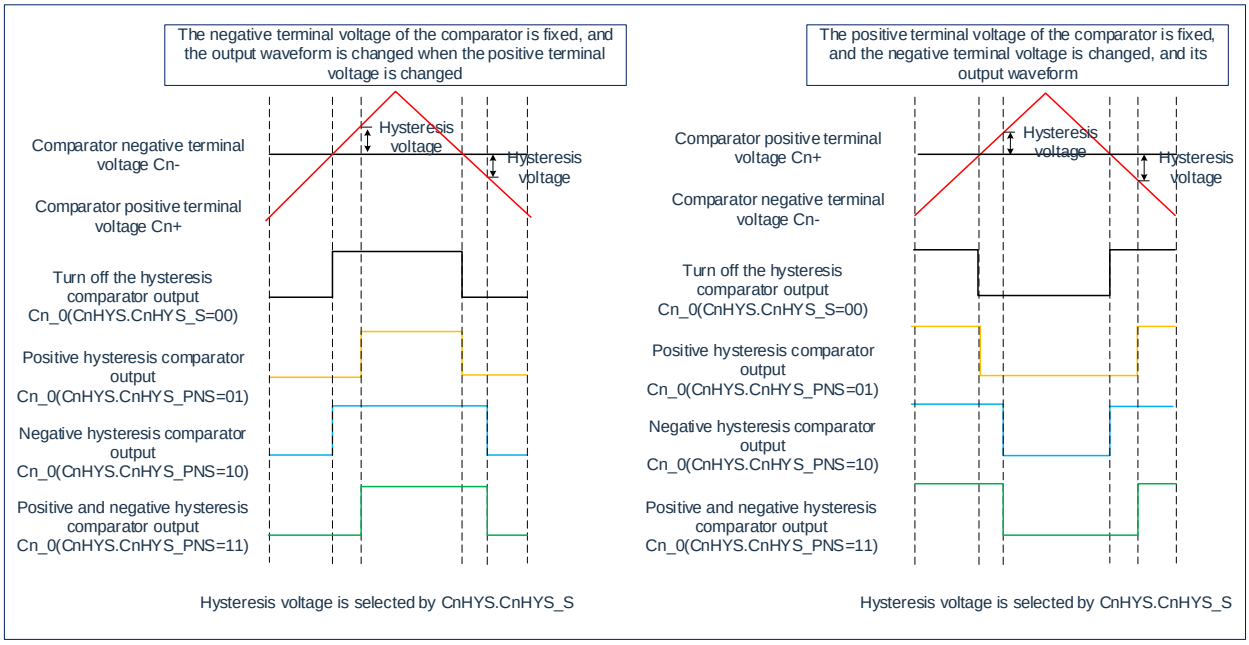


Figure 23-2: Block diagram of the comparator hysteresis function

23.4 Register mapping

(ACMP base address = 0x4D00_0000). RO: read-only, WO: write-only, R/W: read-write

register	Offset	Read/write	description	Reset value
C0CON0(P1B)	0x000	R/W	Analog comparator 0 control register 0	0x0
C0CON1(P1B)	0x004	R/W	Analog comparator 0 control register 1	0x10
C0CON2(P1B)	0x008	R/W	Analog comparator 0 control register 2	0x0
C0ADJE(P1B)	0x00C	R/W	Analog comparator 0 adjust enable register	0x0
C1CON0(P1B)	0x010	R/W	Analog comparator 1 control register 0	0x0
C1CON1(P1B)	0x014	R/W	Analog comparator 1 control register 1	0x10
C1CON2(P1B)	0x018	R/W	Analog comparator 1 control register 2	0x0
C1ADJE(P1B)	0x01C	R/W	Analog comparator 1 adjust enable register	0x0
CVRCON(P1B)	0x020	R/W	Analog comparator reference voltage control register	0x0
CVECON(P1B)	0x024	R/W	Analog comparator event control register	0x0
IMSC(P1B)	0x028	R/W	Analog comparator interrupt enable register	0x0
RICE	0x02C	RO	The analog comparator interrupt source status register	0x0
PUT	0x030	RO	The analog comparator enabled interrupt status register	0x0
ICLR	0x034	WO	Analog comparator interrupt clear register	0x0
LOCK	0x038	R/W	Analog comparator write enable register	0x0

Note:

1) The registers marked (P1B) are protected registers.

2) (P1B): When LOCK==55H, the labeled register is allowed to write; = Other values, forbidden to write.

23.5 Register description

23.5.1 Analog comparator n control register 0 (CnCON0) (n=0-1)

bit	symbol	description	Reset value
31:16	-	reserved	-
15	Cnen	Analog comparator n enable bit 0: Disable 1: Enable	0
14	CnCOFM	Analog comparator n adjustment mode enable bit 0: Disable 1: Enable, positive and negative internal shorts	0
13	CnN2GND	Analog comparator n adjustment mode negative ground enable bit 0: Disable 1: Enables, the positive and negative ends are internally shorted, and the internal ground is grounded (Effective when CnCOFM=1 and CnCRS=0).	0
12:8	-	reserved	-
7:4	CnPS	Analog comparator n positive channel selection bit 000: CnP0 port 001: CnP1 port 010: CnP2 port 011: CnP3 port 100: OP0_O port 101: OP1_O port 110: A0O port 111: A1O port	0
3:0	CnNS	Analog comparator n negative channel selection bit 00: CnN 01: Vref (Bandgap or k*VDD) 1x: forbidden	0

23.5.2 Analog comparator n control register 1 (CnCON1) (n=0-1)

bit	symbol	description	Reset value
31:10	-	reserved	-
9	CnOUT	Analog comparator n result bits (Read-only).	0
8	CnCRS	Analog comparator n mode input selection bit (effective when Cn COFM=1). 0: Negative side 1: Positive end	0
7:5	-	reserved	-
4:0	CnADJ	Analog comparator n adjustment bit	0x10

23.5.3 Analog comparator n control register 2 (CnCON2) (n=0-1)

bit	symbol	description	Reset value
31:14	-	reserved	-
13:12	CnHYSLS	Analog comparator n hysteresis mode control bit 00: No hysteresis 01: Positive hysteresis 10: Negative hysteresis 11: Bilateral hysteresis See the corresponding block diagram in the function description	0
11:10	CnHYSVS	Analog comparator n hysteresis voltage selection (invalid in regulation mode). 00: No lag 01: 10mV 10: 20mV 11: 60mV	0
9	CnPOS	Analog comparator n output polarity select bit 0: Normal output 1: Inverting output	0
8	CnFE	Analog comparator n output filtering enable bit 0: Disable 1: Enable	0
7:4	-	reserved	-
3:0	CnFS	Analog comparator n output filtering time selection bit 0000: (0~1)*Tpclk 0001: (1~2)*Tpclk 0010: (2~3)*Tpclk 0011: (4~5)*Tpclk 0100: (8~9)*Tpclk 0101: (16~17)*Tpclk 0110: (32~33)*Tpclk 0111: (64~65)*Tpclk 1000: (128~129)*Tpclk 1001: (256~257)*Tpclk 1010: (512~513)*Tpclk Other: (0~1)*Tpclk	0

23.5.4 Analog comparator n adjust enable register (CnADJE) (n=0-1)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	CnADJE	AAH: This is determined by the OPnADJ < 4:0 > in the CnCON1 register Other: Determined by the CONFIG related bit	0

23.5.5 Analog comparator reference voltage control register (CVRCON)

bit	symbol	description	Reset value
31:6	-	reserved	-
5:4	CSVR	Analog comparator negative reference voltage selection bit 0x: Choice 1.2V (Bandgap) 10: Select k*VDD 11: Select k*1.2V(0.12V~1.02V)	0
3:0	CVS	Analog comparator reference voltage divider k select bit 0000: 2/20 0001: 3/20 … 1111: 17/20 Note: ◆ The Step for the VDD divider was VDD (1/20). ◆ Choose a Step with a 1.2V divider for 60mV	0

23.5.6 Analog Comparator Event Control Register (CEVCON)

bit	symbol	description	Reset value
31:6	-	reserved	-
5	EVE1	Analog comparator 1 event output enable bit (does not affect interrupt generation) 0: Disable 1: Enable	0
4	EVE0	Analog comparator 0 event output enable bit (does not affect interrupt generation). 0: Disable 1: Enable	0
3:2	EVS1	Analog Comparator 1 events generate conditional selection bits 00: Comparator 1 outputs a jump from 0->1 01: Comparator 1 outputs a jump from 1->0 10: Comparator 1 outputs a jump from 0->1 or a transition from 1->0 11: reserved	0
1:0	EVS0	Analog comparator 0 events produce conditional selection bits 00: Comparator 0 outputs a jump from 0->1 01: Comparator 0 outputs a jump from 1->0 10: Comparator 0 outputs a jump from 0->1 or a transition from 1->0 11: reserved	0

23.5.7 Analog comparator interrupt enable register (IMSC)

bit	symbol	description	Reset value
31:2	-	reserved	-
1	EN_C1IF	Analog comparator 1 interrupt enable bit 0: Disable 1: Enable	0
0	EN_C0IF	Analog comparator 0 interrupt enable bit 0: Disable 1: Enable	0

23.5.8 Analog comparator interrupt source status register (RIS)

bit	symbol	description	Reset value
31:2	-	reserved	-
1	RIS_C1IF	Analog Comparator 1 interrupt source state bit 0: No interrupt was generated 1: An interrupt has been generated (event generation).	0
0	RIS_C0IF	Analog comparator 0 interrupt source status bit 0: No interrupt was generated 1: An interrupt has been generated (event generation).	0

23.5.9 Analog comparator enabled interrupt source status register (MIS)

bit	symbol	description	Reset value
31:2	-	reserved	-
1	MIS_C1IF	Analog Comparator 1 enabled interrupt state bit 0: No interrupt was generated 1: An interrupt has been generated	0
0	MIS_C0IF	Analog comparator 0 enabled interrupt state bit 0: No interrupt was generated 1: An interrupt has been generated	0

23.5.10 Analog comparator interrupt clear control register (ICLR).

bit	symbol	description	Reset value
31:2	-	reserved	-
1	ICLR_C1IF	Analog comparator 1 interrupt clear control bit Write 0: Does not affect Write 1: Clear the RIS_ the C1IF flag bit	0
0	ICLR_C0IF	Analog comparator 0 interrupt clear control bit Write 0: Does not affect Write 1: Clear the RIS_ the C0IF flag bit	0

23.5.11 Analog comparator write enable control register (LOCK).

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of acMP-related registers (See ACMP register mapping for details). When LOCK=other values, operation of ACMP-related registers is prohibited	0

24. Temperature Sensor (TS)

The chip has its own temperature sensor, which can test the output temperature-dependent analog (voltage) through the internal channel of ADC0 or ADCB, and the trimming of the temperature sensor can be selected from the factory configuration, or the user can set it himself. The temperature sensor configuration is set via register LVDCON, and the configuration of ADC0/ADCB is described below.

24.1 Temperature sensor setup process

If the trimming of the temperature sensor is selected from the factory configuration, the temperature detection setting process is as follows:

1) Set temperature sensor detection enable LVDCON[11]=1, trim control select factory-adjusted LVDCON[10]=0;
2) Set the temperature detection channel (channel 17 of the ADC);
3) Set ADC-related configuration registers;
4) Turn on ADC conversion enable;
5) Wait for the ADC conversion to complete and read the register data.

At room temperature, if the trimming of the temperature sensor is set by register LVDCON [9:6], the trimming setting process is as follows:

1) Set temperature sensor detection to enable LVDCON[11]=1, trim control selection LVDCON[9:6]adjust LVDCON[10]=1;
2) Setting the temperature sensor trimming LVDCON [9:6];
3) Set the temperature detection channel (channel 17 of the ADC);
4) Set ADC-related configuration registers;
5) Turn on ADC conversion enable;
6) Wait for the ADC conversion to complete and read the register data;
7) Change the temperature sensor trimming (trimming from 0000 to 1111) and read the ADC output register data until the temperature sensor output is adjusted to 1V.

When measuring temperature sensors, it is recommended to set the sampling rate of the ADC to less than 100Ksps.

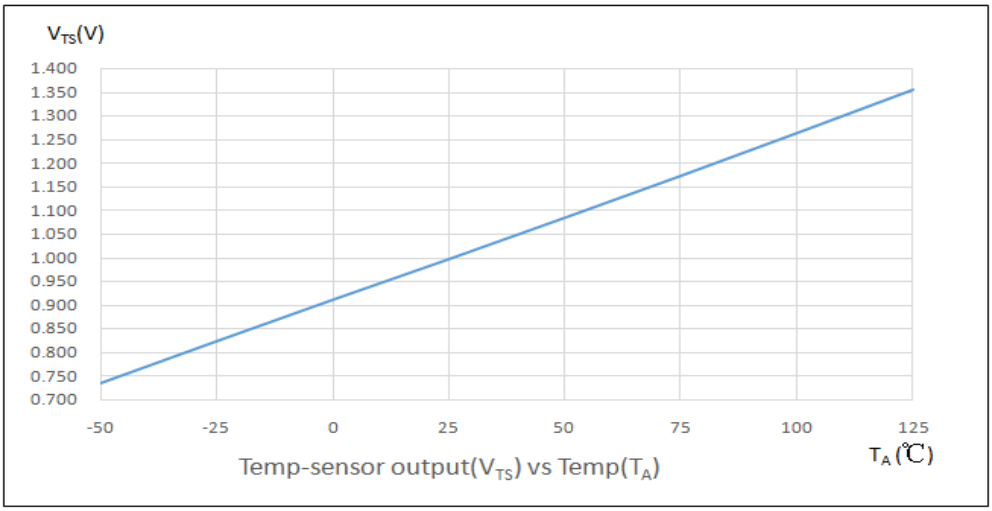
24.2 Description of the sensitivity of the temperature sensor

The analog output voltage of the temperature sensor increases with the temperature of the chip, the analog output voltage is collected by ADC0 and ADCB, converted into a 12-bit digital quantity, according to the conversion result, and then calculated by the corresponding formula, the temperature data of the chip can be obtained.

1) When the temperature changes from -40°C to 105°C, the analog signal voltage range is: 0.7V~1.4V;
2) When the temperature changes from -40 °C to 105 °C, the slope of the analog amount changes with temperature: K: 3.5±0.2 mV/°C;
3) When the temperature is 25°C, the voltage value is: 1±0.01V;
4) The analog signal is approximately linear with temperature, and the change curve is shown in the following figure. In the figure below,T_A is the temperature (unit, °C) and V_{TS} is the output voltage (unit, V) of the temperature sensor.

Temp-sensor output(V_{TS}) vs Temp(T_A)

T_A	-50	-25	0	25	50	75	100	125
V_{TS}	0.734	0.821	0.909	0.997	1.085	1.173	1.263	1.354



24.3 Temperature sensor conversion formula

The result of the temperature sensor conversion is:

$$RES_{AD}=\frac{V_{TS}}{V_{REF}}\times 4096$$

Where theRES_{AD} measured 12-bit AD conversion value is the reference voltage of the ADC (in VV_{REF}) and the output voltage of the analog signal (inV_{TS} V). ΔV is analog signal output voltage.

The temperature (T) calculation reference formula is as follows:

$$T=(\frac{V_{REF}\times RES_{AD}}{4096}-0.909)\div K$$

where K is the slope of the analog quantity with temperature (unit, V/°C).

25. Memory Control Module (FMC)

25.1 overview

Up to 64KB on-chip flash for storing applications. A user configuration area for system initialization. Supports application programming (IAP), after updating the flash program, when performing a switch between the bootloader and the user program, there is no need for external reset.

25.2 characteristic

- Supports up to 64KB of application storage space (APROM).
- Support BOOT function, BOOT area and APROM share a maximum of 64KB space, the size can be set 1KB/2KB/4KB.
- Supports a 1KB data storage area and does not take up program space.
- Supports 512-byte page erase for all on-chip Flash operations.
- Supports On-Chip Programming (ISP)/In-Application Programming (IAP) to update on-chip Flash.
- Supports CRC checksum calculation and detection of program space codes of any interval.

25.3 Feature description

25.3.1 Memory structure

The on-chip FLASH contains a maximum of 64KB user program area (APROM) and 512 Byte user configuration area (User Configuration).

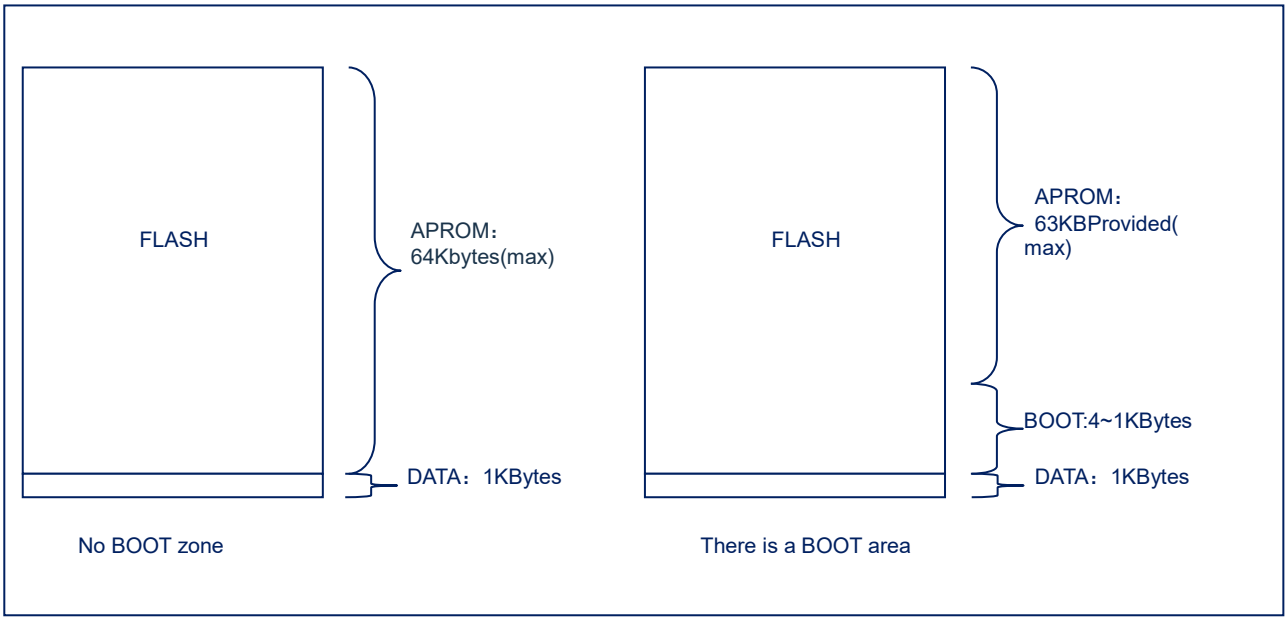


Figure 25-1: Storage structure diagram

25.3.2 Flash's operation

Erase: Includes two commands: overall erase and page erase.

1) When erased as a whole, the entire APROM space is erased. The overall erase operation method is as follows:
   - Enables access to FMC-related registers.
   - Wait for the FMC to idle.
   - Writes 0x06 in FMCCMD.
   - Wait for the FMC to idle.
   - Disable access to FMC-related registers.

2) When a page is erased, each page can erase 0x200 address space. Here's how to do page erasure:
   - Enables access to FMC-related registers.
   - Write the page erase header address in FMCADR.
   - Wait for the FMC to idle.
   - Writes 0x03 in FMCCMD.
   - Wait for the FMC to idle.
   - Disable access to FMC-related registers.

Programming: After the erase is complete, the page data can be programmed continuously. The programming is as follows:

1) Enables access to FMC-related registers.
2) Set the address that needs to be programmed in FMCADR.
3) Write the data that needs to be programmed in FMCDAT.
4) Wait for the FMC to idle.
5) Writes 0x02 in FMCCMD.
6) Wait for the FMC to idle.
7) Disable access to FMC-related registers.

Read: Contains two ways to read:

1) Direct addressing, which directly reads the 0x0000-0x7FFF address.
2) Read by FMC command, the operation sequence is as follows:
   - Enables access to FMC-related registers.
   - Set the address to be read in FMCADR.
   - Writes 0x01 in FMCCMD.
   - Read the FMCDAT value.
   - Disable access to FMC-related registers.

25.3.3 Flash space CRC check

See < security-related > sections for details.

25.3.4 Flash space program startup selection

The chip can be configured to boot from APROM or from the BOOT zone after power-on reset. The relevant selections are selected in the user configuration area:

BOOT_TYPE	Power-on boot selection instructions
1111	Boot from APROM
0001	Boot from theBOOT area
0000	Booting from theBOOT region requires theBOOT pin to be grounded
other	Boot from APROM

If you need to boot from BOOT, you need to allocate a valid space to the BOOT area: 1KBytes/2KBytes/4KBytes.

If the space allocated by BOOT is 0KBytes, even if BOOT_TYPE chooses to start from the BOOT area, it is actually started from APROM.

After choosing to start from the BOOT area to complete the bootloader, if you need to go to APROM program execution, it is recommended to perform the following steps:

1) Write the ISPS bit of the FMCCON register to 1, allowing the next reset procedure to be executed from APROM.
2) Write the RSTCON register to 0x55aa669a, allowing the system to reset (without reloading the boot configuration).
3) After the system resets, the program will be executed from the APROM area.

After the program is run in APROM, if it is necessary to go to the BOOT area for execution, it is recommended to perform the following steps:

1) Write the ISPS bit of the FMCCON register to 0, allowing the next reset procedure to be executed from the BOOT area.
2) Write the RSTCON register to 0x55aa669a, allowing the system to reset (without reloading the boot configuration).
3) After the system resets, the program will be executed from the BOOT area.

25.4 Register mapping

(FMC base address = 0x4980_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/ write	description	Reset value
CON(P1D)	0x000	R/W	FMC control register	-
ADR(P1D)	0x004	R/W	FMC address register (FMC CRC checks the start address register).	0x0
DAT(P1D)	0x008	R/W	FMC data register	0x0
CMD(P1D)	0x00C	R/W	FMC command register	0x0
LOCK	0x010	R/W	FMC access enable register	0x0
CRCEA(P1D)	0x020	R/W	FMC CRC checksum end address register	0xFFFF
CRCIN(P1D)	0x024	R/W	FMC CRC input register	0x0
CRCD(P1D)	0x028	R/W	FMC CRC data register	0x0

Note:

1) The registers marked (P1D) are protected registers.
2) (P1D): Lock==55AA6699H, the marked register is allowed to write; = Other values, forbidden to write.

25.5 Register description

25.5.1 FMC Control Register (CON)

bit	symbol	description	Reset value
31:6	-	reserved	-
5	BUSY	FMC busy flag bit 0: FMC idle 1: The FMC is busy and performs erase, programming, or reading operations normally	0
4	ISPS	Select the location where the program starts after the next reset (Excluding power-on reset, MCURST reset, external reset). 0: After reset, the program is executed from BOOT (BOOT region and BOOT enable need to be configured). 1: After the reset the procedure is performed from the APROM	1
3:0	-	reserved	-

25.5.2 FMC Address Register (ADR)

bit	symbol	description	Reset value
31:0	ADDR[31:0]	The word operation address (or the starting address of the CRC check operation). 0x00xx_xxxx（is APROM） 0x1cxx_xxxx (is DATA region) (The lower two digits must be 00).	0

25.5.3 FMC Data Register (DAT)

bit	symbol	description	Reset value
31:0	FMCDAT	When a write operation is performed, the data is written to FLASH, and when a read operation is performed, the FLASH data is returned	0

25.5.4 FMC Command Register (CMD)

bit	symbol	description	Reset value
31:5	-	reserved	-
4:0	FMCFUNC	FMC features 0x0: reserved 0x1: Read the data 0x2: Write data (50us). 0x3: Page erase (4.6ms). 0xD: CRC check（CRC16-CCITT） Other: reserved	0

25.5.5 FMC access enable register (LOCK)

bit	symbol	description	Reset value
31:0	FMCLOCK	Writes 0x55AA6699 enables accessing the other FMC registers; read value is 1 Write any other value, disable the operation of other FMC registers, and read value is 0	0

25.5.6 FMC CRC checksum end address register (CRCEA)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:0	CRCEA	The CRC checksum end address	0

25.5.7 FMC CRC Input Register (CRCIN)

bit	symbol	description	Reset value
31:8	-	reserved	-
7:0	CRCIN	The CRC input requires 8 bits of data to be calculated	0

25.5.8 FMC CRC Data Register (CRCD)

bit	symbol	description	Reset value
31:16	-	reserved	-
15:0	CRCD	The CRC holds the 16-bit result of the operation	0

26. Security-related

26.1 overview

The chip supports functions related to code security and application security.

26.2 Unique Chip Identification Number (UID).

Each chip has a different 96-bit unique identification number, or Unique identification. It has been set at the factory and cannot be modified by the user. The chip UID is read through the memory module when used(this function requires the support of the relevant CMS departments).

There are two ways to read UIDs:

1) Read by the FMC module, the corresponding address mapping is as follows:

(Memory base address = 0x1800_0000) RO: read-only; WO: Write only; R/W: Read and write.

address	Offset	Read/write	description	Reset value
Reserved	0x000	-	reserved	-
UID0	0x004	RO	UID[31:0]	-
UID1	0x008	RO	UID[63:32]	-
UID2	0x00C	RO	UID[95:64]	-

2) Read by the system control module SYSCON, the corresponding address mapping is as follows:

(Register base address = 0x5000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
Reserved	0x000	-	reserved	-
CIDL	0x034	RO	UID[63:32]	-
YES	0x038	RO	UID[95:64]	-
UIDX	0x500	RO	UID[31:0]	-

26.3 User Unique Chip Identification Number (USRUID)

The chip has another 128-bit chip identification number USRUID. Includes a 96-bit user-programmable identification number and a 32-bit fixed identification number, which is distinguished from the UID by the fact that it is not readable in the USRUID program. The user can set the unique 96-digit identification number in the CMS tool. Of which the other 32bit is not operational.

The 128-bit USRUID can be used as a key in an encryption application, the user program can detect the key to establish a protection mechanism.

Mechanism to prevent decryption operation in the program: If the detection result is incorrect, the USRUID detection is immediately disabled, the re-detection operation will be ignored, only after a reset detectoion can be activated again, and the single detection tolerance rate is 0.

USRUID has a separate encryption bit in the User Configuration area, and after setting the USRUID to the encryption state, no other method or tool can read out the data in it.

The specific methods of detection are as follows:

At the same time, there are 4 registers in the system control module, namely UUIDWC0, UUIDWC1, UUIDWC2, UUIDWCS is used to detect USRUID data if written to UUIDWC0-U UIDWC2 (write 96bit user identification number), UUIDWCS (must write 0xFFFFFFFFFF) All data is the same as the data of the preset USRUID, the values of these registers are read as 0x1, otherwise it is 0.

The mechanism of decryption operation in the program: If the data written is incorrect, the USRUID detection operation is immediately disabled, and the operation of writing to the USRUID again will be ignored, and it needs to be reset to detect again, and the fault tolerance rate of a single detection is 0.

26.4 Protection of program code

The chip supports the protection function of the chip code and the code partition protection function.

APROM partition protection: The 64KBytes space is divided into 32 segments, each with a size of 2KBytes, CFG_APROMPE the user configuration register The protection status can be set individually. If a BOOT interval has been assigned, the protection state acts into the valid region.

APROM protection status description												
bit	address	Valid status	Read			programming			Erase			Default value
			NM	SW	BT	NM	SW	BT	NM	SW	BT	-
0	0x0000-0x07FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
1	0x0800-0x0FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
2	0x1000-0x17FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
3	0x1800-0x1FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
4	0x2000-0x27FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
5	0x2800-0x2FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
6	0x3000-0x37FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
7	0x3800-0x3FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
8	0x4000-0x47FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
9	0x4800-0x4FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
10	0x5000-0x57FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
11	0x5800-0x5FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
12	0x6000-0x67FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
13	0x6800-0x6FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
14	0x7000-0x77FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
15	0x7800-0x7FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
16	0x8000-0x87FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
17	0x8800-0x8FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
18	0x9000-0x97FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
19	0x9800-0x9FFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
20	0xA000-0xA7FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
21	0xA800-0xAFFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
22	0xB000-0xB7FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
23	0xB800-0xBFFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
24	0xC000-0xC7FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
25	0xC800-0xCFFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
26	0xD000-0xD7FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
27	0xD800-0xDFFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
28	0xE000-0xE7FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
29	0xE800-0xEFFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
30	0xF000-0xF7FF	0	✓	×	✓	×	✓	✓	×	✓	✓	1
31	0xF800-0xFFFF	0	✓	×	✓	×	✓	✓	×	✓	✓	1

NM = Normal

SW = SWD status

BOOT = BOOT status

BOOT partition protection: The 4KBytes space is divided into 4 segments, each segment is 1KBytes, and the protection status can be set separately in the user configuration register CFG_BOOTPE. If an APROM interval has been assigned to it, the protection state acts within the valid BOOT region.

Description of the boot area protection status												
bit	address	Valid status	Read			programming			Erase			Default value
			NM	SW	BT	NM	SW	BT	NM	SW	BT	-
0	0xF000-0xF3FF	0	×	×	✓	×	×	×	×	×	×	1
1	0xF400-0xF7FF	0	×	×	✓	×	×	×	×	×	×	1
2	0xF800-0xFBFF	0	×	×	✓	×	×	×	×	×	×	1
3	0xFC00-0xFFFF	0	×	×	✓	×	×	×	×	×	×	1

NM = Normal

SW = SWD status

BOOT = BOOT status

26.5 Procedure CRC check

26.5.1 CRC checksum calculation for Flash space

The chip supports the hardware calculation program CRC checksum. The FMC control module supports hardware to automatically calculate the value of CRC16. The check interval can be set arbitrarily. The CRC checksum is generated using the polynomial CRC-16-CCITT 'X^{16}+X^{12}+X^{5}+1', The relevant registers are as follows:

FMCADR: The start address register for the CRC check

FMCCRCEA: The end address register for CRC checksum (FMCRCCEA>=FMCADR) is required

FMCCRCIN: Input register for CRC checking

FMCCRCD: Data register for CRC checking (holds 16-bit results of C RC checking).

The steps to calculate the CRC checksum are as follows:

1) Set the starting address of the required check space in FMCADR
2) Set the end address of the required check space in FMCCRCEA, which must be greater than or equal to FMCADR
3) Write FMCCRCIN to 0x00
4) Write FMCCRCD to 0x0000, clear the previous results
5) Write FMCCMD to 0xD and start the CRC checksum
6) After the CRC check is complete, the BUSY bit in FMCCON will be set to 0
7) Read the FMCCRCD data, that is, the calculated CRC checksum

During the Flash space check, the CPU stops, and after the calculation is complete, the CPU continues to run. The CRC check is checked bytely (8 bits), in order from the initial address to the end address.

For example, the data 0x0 address is 12H, the data at address 0x1 is 34H, the data at address 0x2 is 56H, and the data at address 0 x3 is 78 H, the value of CRC is calculated sequentially in the order of 12H->34H->56H->78H, and the final checksum code is: 67F0H

Validating 64Kbytes of program space requires approximately 1.5ms@Fsys=64MHz.

The CRC check of the Flash space takes effect on the absolute address of flash and is not affected by the protected state, the BOOT state.

26.5.2 CRC checksum comparison for Flash space

The program CRC checksum is recommended to be generated using the polynomial CRC-16-CCITT of "X^{16}+X^{12}+X^{5}+1". This uses the same polynomial in the CRC module in FMC to quickly verify that the program code is correct. (CMS-related tool support is required when using this function).

There are two ways to read PCRCD:

- Read by the FMC module, the corresponding address mapping is as follows:

(Memory address = 0x1000_0000) RO: read-only; WO: Write only; R/W: Read and write.

address	Offset	Read/write	description	Reset value
PCRCD	0x01C	RO	PCRCD	-

- Read by the system control module SYSCON, the corresponding address mapping is as follows:

(Register base address = 0x5000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
PCRCD	0x510	RO	{ 16'h0，PCRCD }	-

26.6 CRC operation (general CRC).

The universal CRC module is used to verify the correctness of the program or data transmission. The CRC operations of the general-purpose module operate at the APB clock.

The polynomial of CRC is "X 16+X 12+X^5+1" of CRC-16-CCITT.

26.7 Memory illegal access detection

Access to the illegal memory address in the ARM microcontroller generates an error exception, which provides a better method of detecting program errors and allows software errors to be detected earlier.

In an AHB system connected to a Cortex-M0 processor, the address resolution logic probes for the address being accessed, and if an illegal location is being accessed, the bus system responds with an error signal that can cause a bus error by taking values or data access.

26.8 SRAM protection function

The on-chip SRAM is write-protected and can be set to zonal write-protected. Write protection does not affect the read function, the system register SRAMLOCK can set the relevant function.

26.8.1 SRAM write enable register (SRAMLOCK)

bit	symbol	description	Reset value
31:16	LOCK	When LOCK=0x55AA, the write protection of SRAM takes effect	0x0
15:4	--	reserved	0x0
3:0	REGION	Bit3: Set the SRAM address 0x20001800-0x20001FFF area to a write-protected state Bit2: Set the SRAM address 0x20001000-0x200017FF area to write-protected Bit1: Set the SRAM address 0x20000800-0x20000FFF area to write-protected Bit0: -- Write 0 to disable protection (read/write). Write 1 to enable protection (read only allowed). Note: The 2KBytes area with an initial address range of 0x20000000-0x2000 07FF is free to read and write.	0x0

26.9 SFR protection function

Some SFRs of the key function modules have protection functions and can be set to level protection. The associated registers with SFR protection can be referred to the register mapping instructions for each module.

The protection level types are as follows:

Protection level	The type of protection	Description
0	P0	While Data is written, detect other register values at the same time (A569H/55AAH).
1	P1A	While Data is written, detect other register values (55H/AAH/99H).
2	P1B	While Data is written, detect other register values (55H).
3	P1C	While Data is written, detect other register values (55AAH).
4	P1D	While Data is written, detect other register values (55AA6699H).
5	P2	Reserved

For example, GPIO, IOCFG, WDT, FMC, CCP0/1, EPWM, ACMP0/1, Function modules such as ADC0/ADCB have similar protection lock registers to implement SFR protection functions. For specific use, please refer to the user manual for each module.

26.10 ADC test function

This A/D test function verifies that the A/D converter is operating properly by converting the A/D converter's positive reference voltage, negative reference voltage, analog input channel (ANi), and internal reference voltage.

26.11 GPIO pin level detection

When the port is configured as a GPIO as the output port, the status of the pin can also be read. That is, it is possible to detect whether the IO port is used as the output port and the preset level value is output correctly. In GPIO function mode, pin levels can be read via GPIO-> DI, regardless of whether the port is configured as an output or an input port.

Each set of GPIO input circuits supports filtering and is selectable in filter width. The GPIOxDIDB register determines whether to filter and the sample clock for filtering. The basic sample clock of the filter is HCLK, and HCLK-HCLK/14 can be selected from a total of 8 sample clock options.

After three consecutive samples by the sample clock, if they are all at the same level, the pin level is considered stable. If it is not the same, the pin level is considered to be jittery, and the read value is the state of the level before jitter. This structure filters out glitches less than 2*Ts (sampling clock cycle) width.

27. User Configuration Area (UCFG)

27.1 overview

The user configuration area is a separate storage area allocated in FLASH, which reserves registers for the system and is used to configure the external reset IO multiplexing function, encryption function, userID and other information.

27.2 Register mapping

(Base address = 0x1000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	Read/write	description	Reset value
Config0	0x000	RO	User configuration register 0	-
Config1	0x004	RO	User configuration register 1	-
Config2	0x010	RO	User configuration register 2	-
Config3	0x014	RO	User configuration register 3	-
INSRUID0	0x024	RO	The user's unique chip identification number ID0	-
INSRUID1	0x028	RO	The user's unique chip identification number ID1	-
INSRUID2	0x02c	RO	The user's unique chip identification number ID2	-

27.3 Register description

27.3.1 User Configuration Register 0 (Config0)

bit	symbol	description	Reset value
31:24	-	reserved	-
23:13	-	reserved	-
12:11	Reset voltage selection bit	Reset voltage selection bit 01: 2.6V 10: 2.1V 11: 1.9V	-
10:8	-	reserved	-
7:4	BOOT_TYPE	Program start position selection on power-on reset (requires allocation of validBOOT space). 1111: - 0011: Boot from APROM 0001: Boot from the BOOT area 0000: Start from the BOOT area, configure the BOOT pin as a dedicated port, and require the BOOT pin = 0. Other: Boot from APROM Note: Booting from the BOOT area requires allocating a valid BOOT space, otherwise booting from APROM.	-
3	-	Must be 0	-
2	USRIDPE	User UID encryption bit 1: Not encrypted 0: encrypted	-
1	-	Must be 1	-
0	DATA-PROTECT	Encryption bits 1: Not encrypted 0: encrypted	-

27.3.2 User Configuration Register 1 (Config1)

bit	symbol	description	Reset value
31:28	CONFIG_EN_WDT	WDT enable bit 1111: Power-on does not enable WDT Other: Power-on enables WDT	-
27:24	WDT_TIME	0000: 2ms（WDTLOAD=0x50） 0001: 4ms（WDTLOAD=0xA0） 0010: 8ms（WDTLOAD=0x140） 0011: 16ms（WDTLOAD=0x280） 0100: 32ms（WDTLOAD=0x500） 0101: 64ms（WDTLOAD=0xA00） 0110: 128ms（WDTLOAD=0x1400） 0111: 256ms（WDTLOAD=0x2800） 1000: 512ms（WDTLOAD=0x5000） 1001: 1024ms（WDTLOAD=0xA000） 1010: 1638ms（WDTLOAD=0xFFFF） 1011: 1638ms（WDTLOAD=0xFFFF） 1100: 1638ms（WDTLOAD=0xFFFF） 1101: 1638ms（WDTLOAD=0xFFFF） 1110: 1638ms（WDTLOAD=0xFFFF） 1111: 1638ms（WDTLOAD=0xFFFF）	-
23:14	-	reserved	-
13:12	DEBUGEN	SWD debug enable bit 00: Disable Other: Enable	-
11:10	RESETIOS	External reset selection 11: External reset prohibits 10: External reset prohibits 01: P54 as an external reset port 00: P07 as an external reset port	-
8	BOOTIOS	BOOT pin select bit (You need to enable the BOOT function and choose to start from the BOOT pin to take effect, otherwise the relevant port is GPIO) 0: P40 acts as a BOOT pin and is active low 1: P03 acts as a BOOT pin and is active low	-
7:0	-	reserved	-

27.3.3 User Configuration Register 2 (Config2)

bit	symbol	description	Reset value
31:0	USRAPE	APROM program space write protection bit (one segment every 2K). If a BOOT region is assigned, then Bit30, Bit31 bits act to the valid APROM region. The protection status is: SWD prohibits read/write/single page erase. Normally disables write/erase. BOOT program operations are not affected Bit0: 0x0000-0x07FF (absolute address of F LASH). Bit1: 0x0800-0x0FFF Bit2: 0x1000-0x17FF …… Bit30: 0xF000-0xF7FF Bit31: 0xF800-0xFFFF 0: protection 1: Not protected	-

27.3.4 User Configuration Register 3 (Config3)

bit	symbol	description	Reset value
31:20	-	reserved	-
19:16	INSRBTS	APROM/BOOT space allocation bits 0000: APROM=60K； BOOT=4K 0001: APROM=62K； BOOT=2K 0010: APROM=63K； BOOT=1K other: APROM=64K； BOOT=0K	-
15:4	-	-	-
3:0	USRBPE	BOOT program space write protection bit (one segment every 1K). If the BOOT region is less than 4K, the protective bit acts on the activeBOOT region. The protection status is: SWD prohibits read/write/single page erase. Normal operation prohibits read/write/erase. The BOOT program prohibits reading/writing/erasing. Bit0: 0xF000-0xF3FF (absolute address of F LASH). Wit1: 0xF400-0xF7FF Bit2: 0xF800-0xFBFF Bit3: 0xFC00-0xFFFF 0: protection 1: Not protected	-

27.3.5 The user's unique chip identification number ID0 (USRUID0).

bit	symbol	description	Reset value
31:0	USRUID0	The user's unique chip identification number ID bit [31:0].	-

27.3.6 The user's unique chip identification number ID1 (USRUID1).

bit	symbol	description	Reset value
31:0	USRUID1	The user's unique chip identification number ID bit [63:32]	-

27.3.7 The user's unique chip identification number ID2 (USRUID2).

bit	symbol	description	Reset value
31:0	USRUID2	The user's unique chip identification number ID bit [95:64].	-

28. Version Revision Notes

Version number	Time	Revision content
V1.00	May 2019	Initial release
V1.01	Apr 2020	Added ADCB External Reference related description Added user configuration area register description Modified APBCKSEL/UARTxEFR/I2CCLK register description
V1.02	Feb 2023	Modify register description
V1.0.3	Mar 2023	Modify 27.3.1 Reset voltage selection bit
V1.0.4	May 2023	1) Modified section 22.4, 22.5.2 2) Deleted the content of the original 22.5.3 op-amp n regulation enable control register
V1.0.5	Jan 2024	1) Modified description of Section 12.3 2) Corrected the cover page
V1.0.6	May 2024	1) Modify the description about sleep mode and deep sleep mode in 4.2 Working Mode and delete the content about Stop mode 2) Modify 5.3.5 Register description 3) Modify 8.2.4 Register description 4) Delete the stop mode in section 9.3.6 5) Modify 9.5.12 Register description
V1.0.7	Sep 2024	1) Corrected 17.3.2 Incorrect content 2) Revised the cover page